



100

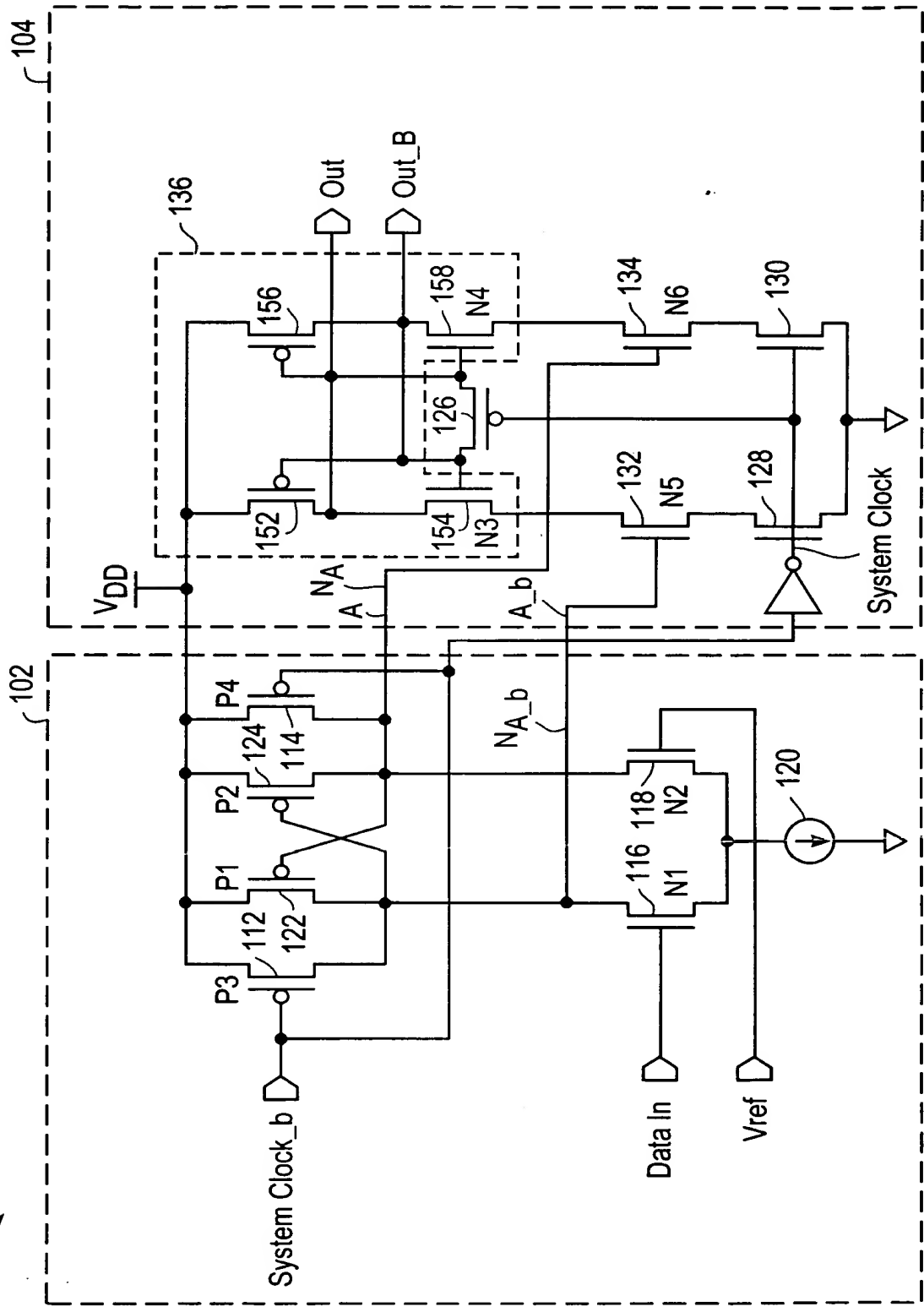


FIG. 1 (Prior Art)

U.S. Patent and Trademark Office  
Washington, D.C. 20540  
Patent No. 6,111,111  
Date of Patent: 10/10/01  
Inventor: John Doe  
Attorney: Jane Smith

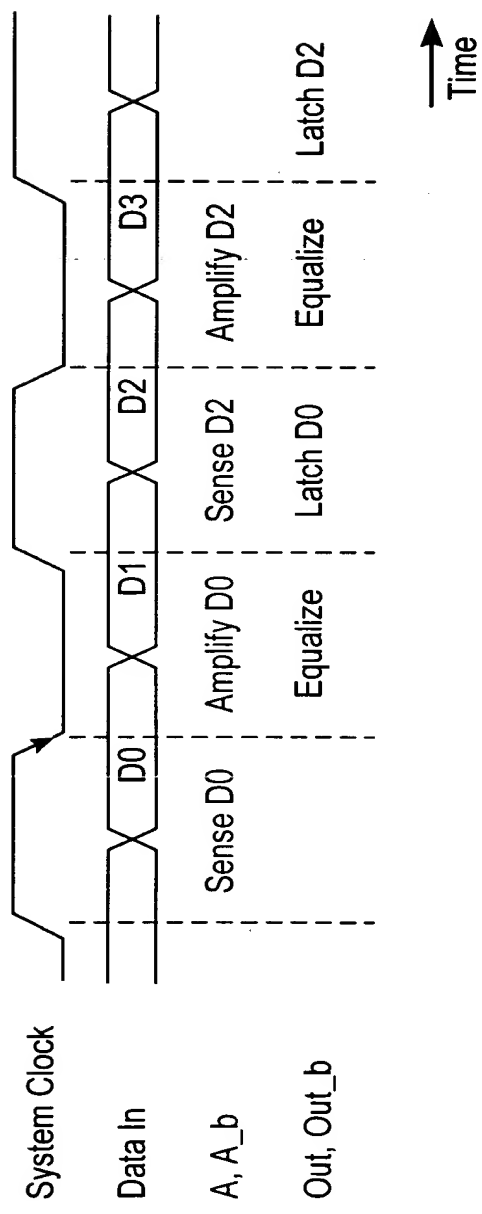


FIG. 2 (Prior Art)

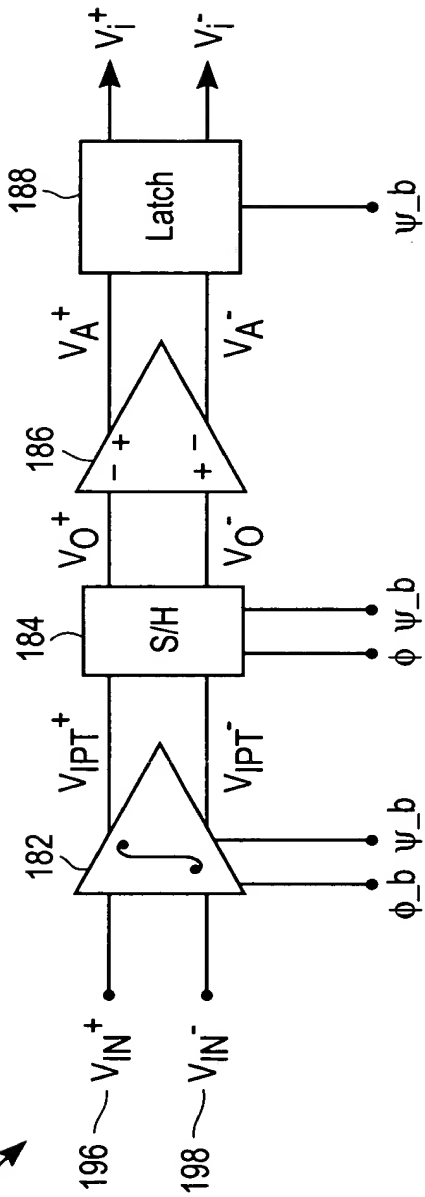


FIG. 3A (Prior Art)

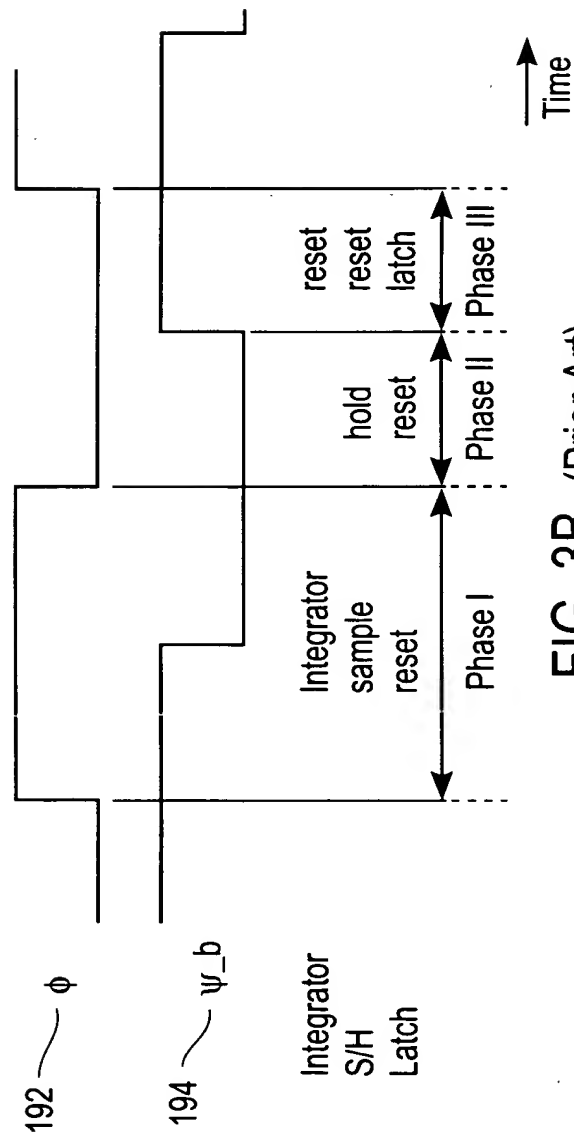
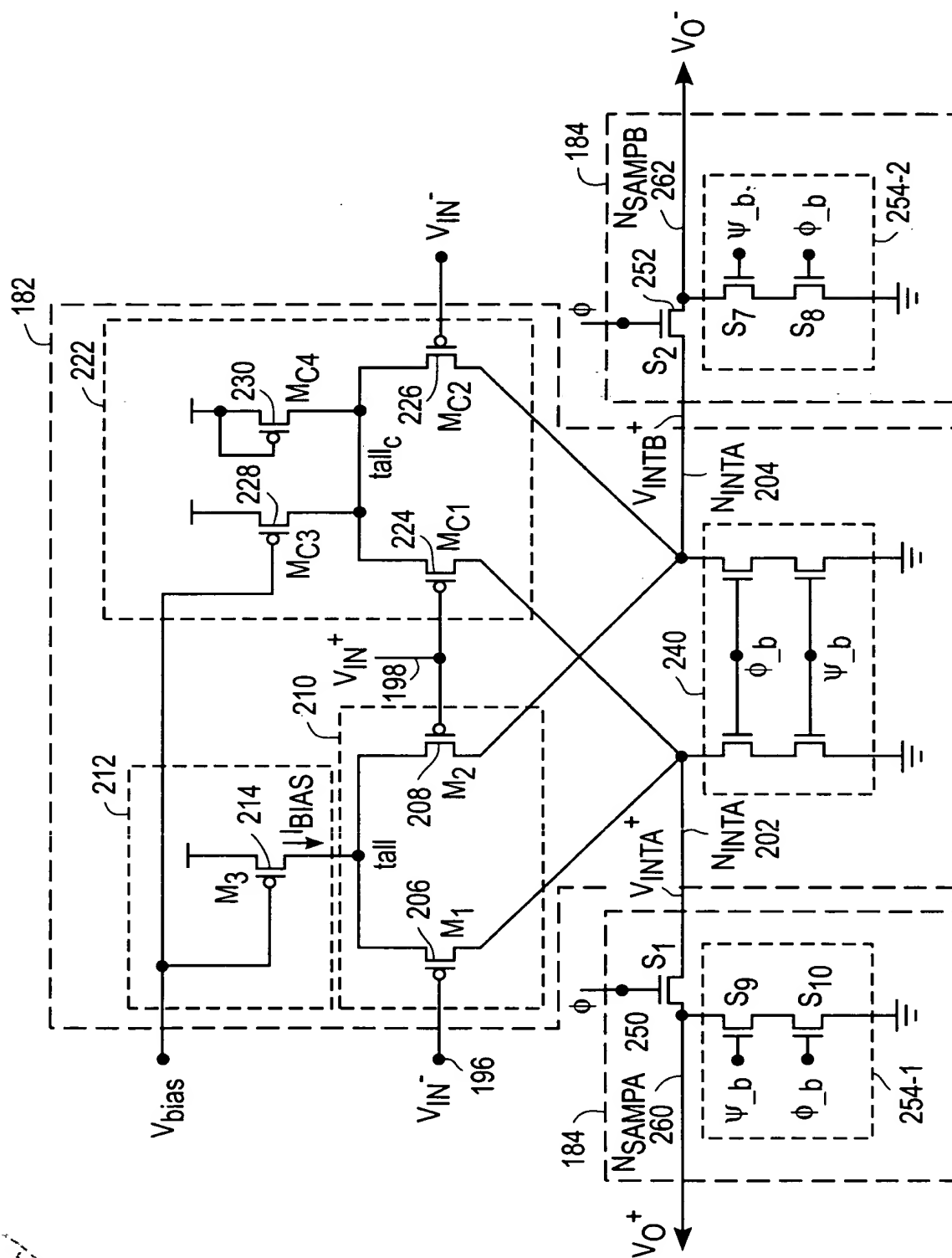


FIG. 3B (Prior Art)



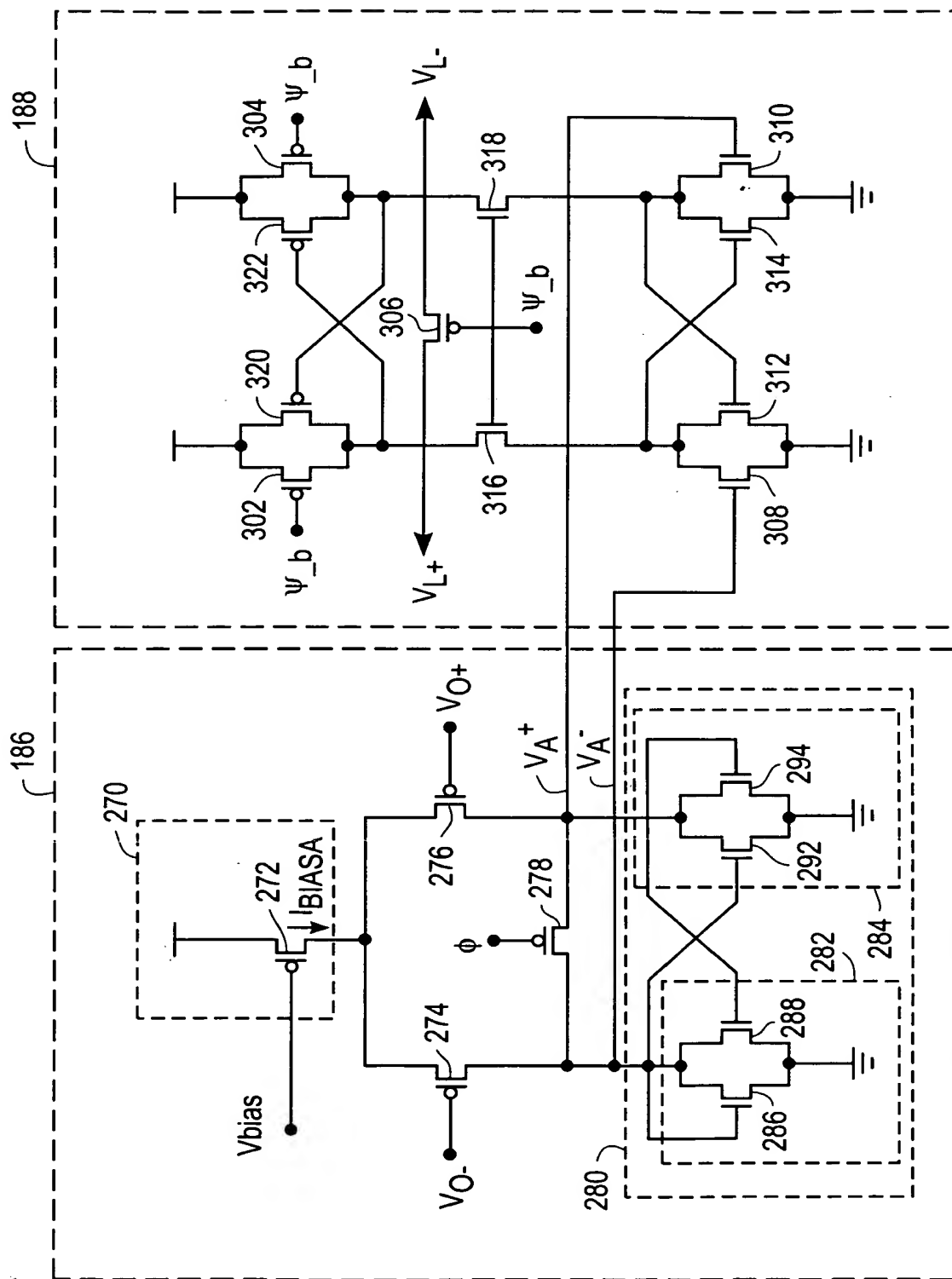


FIG. 5 (Prior Art)

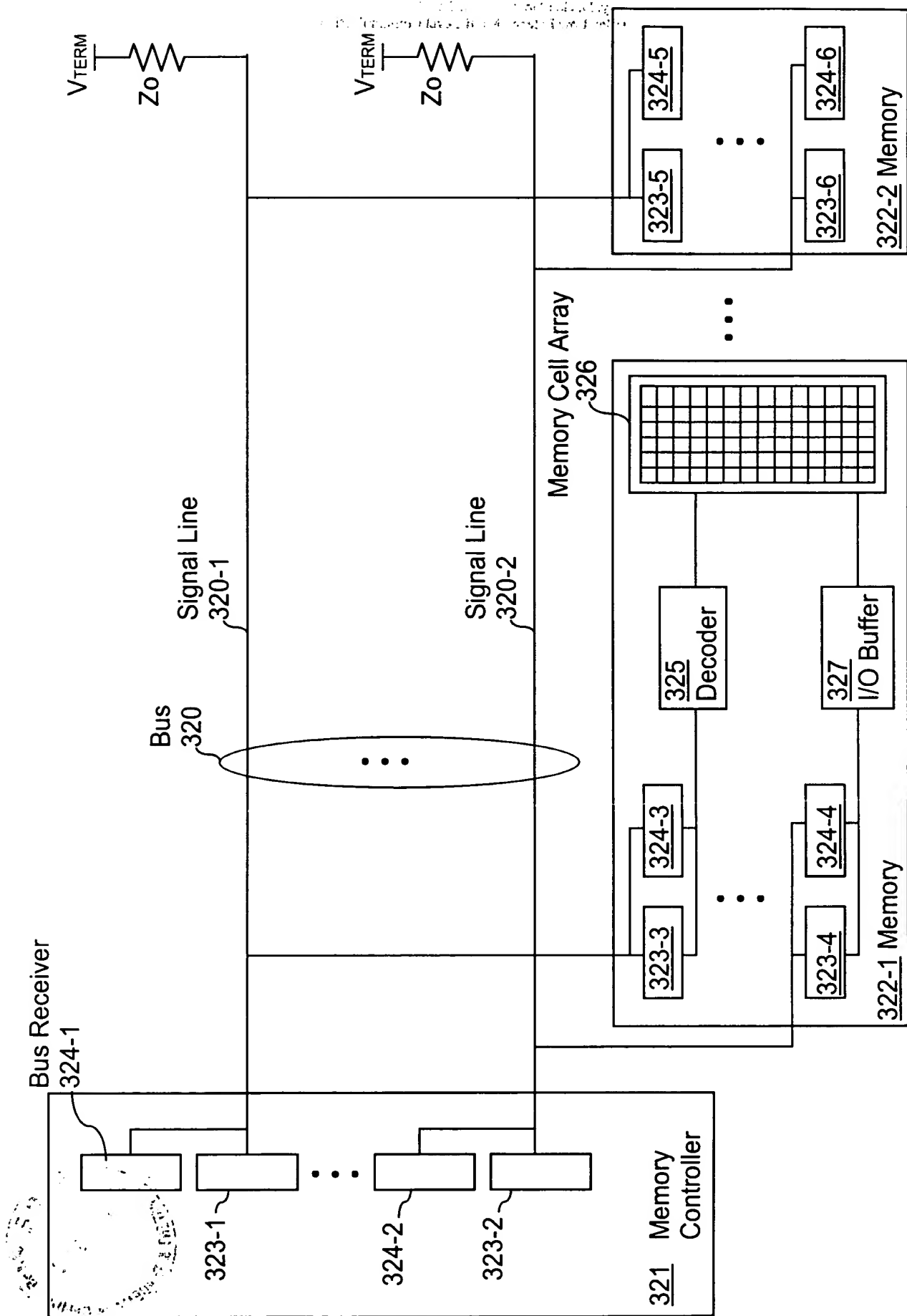


FIG. 6

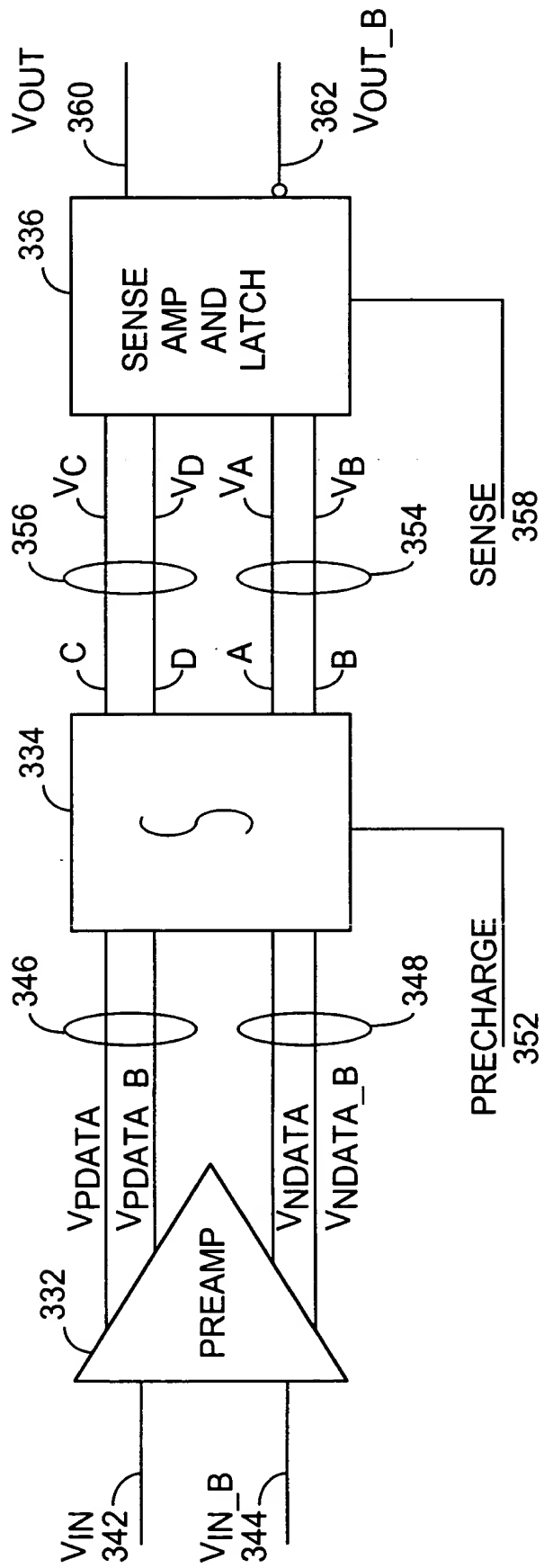


FIG. 7A

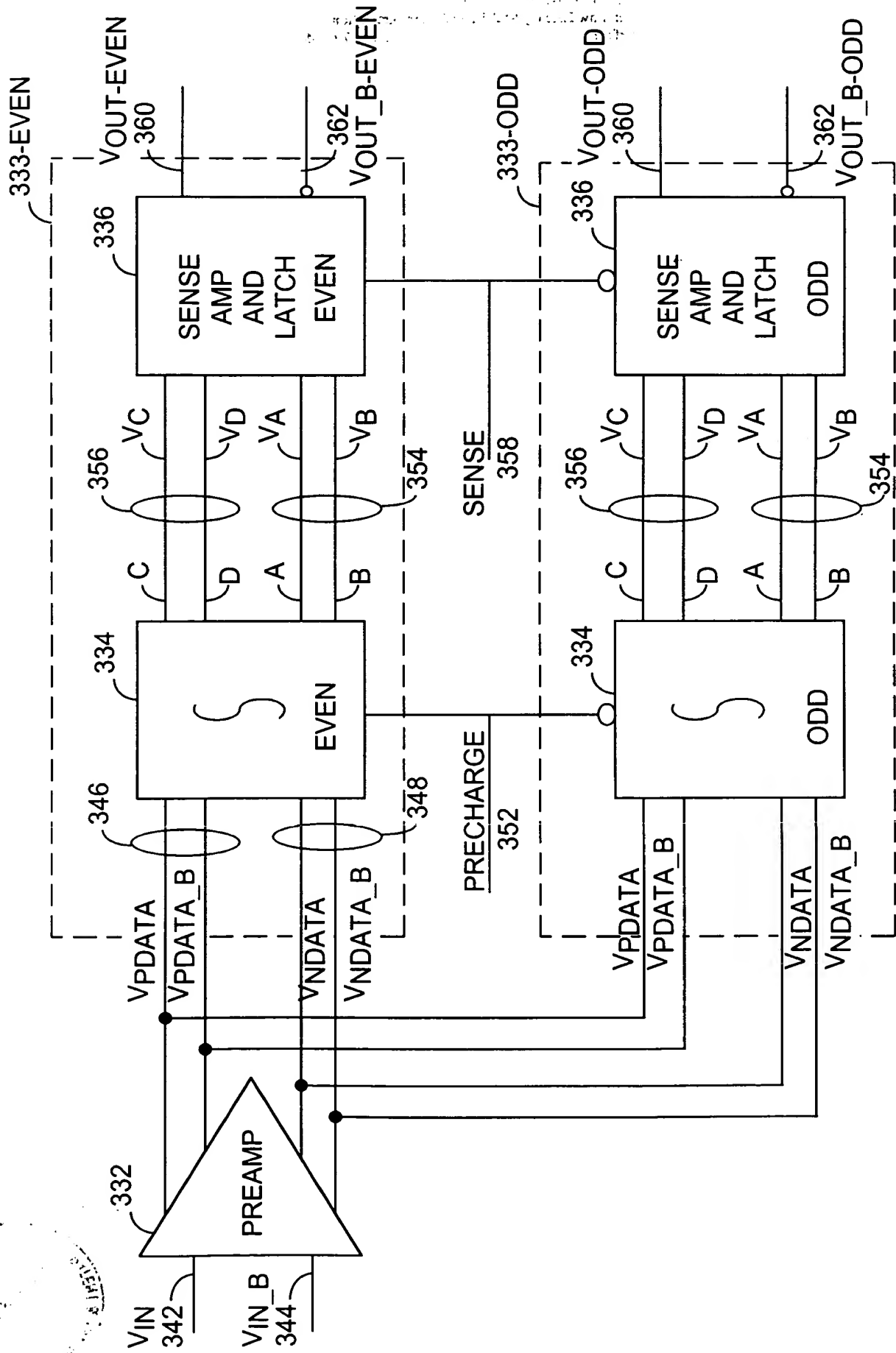


FIG. 7B

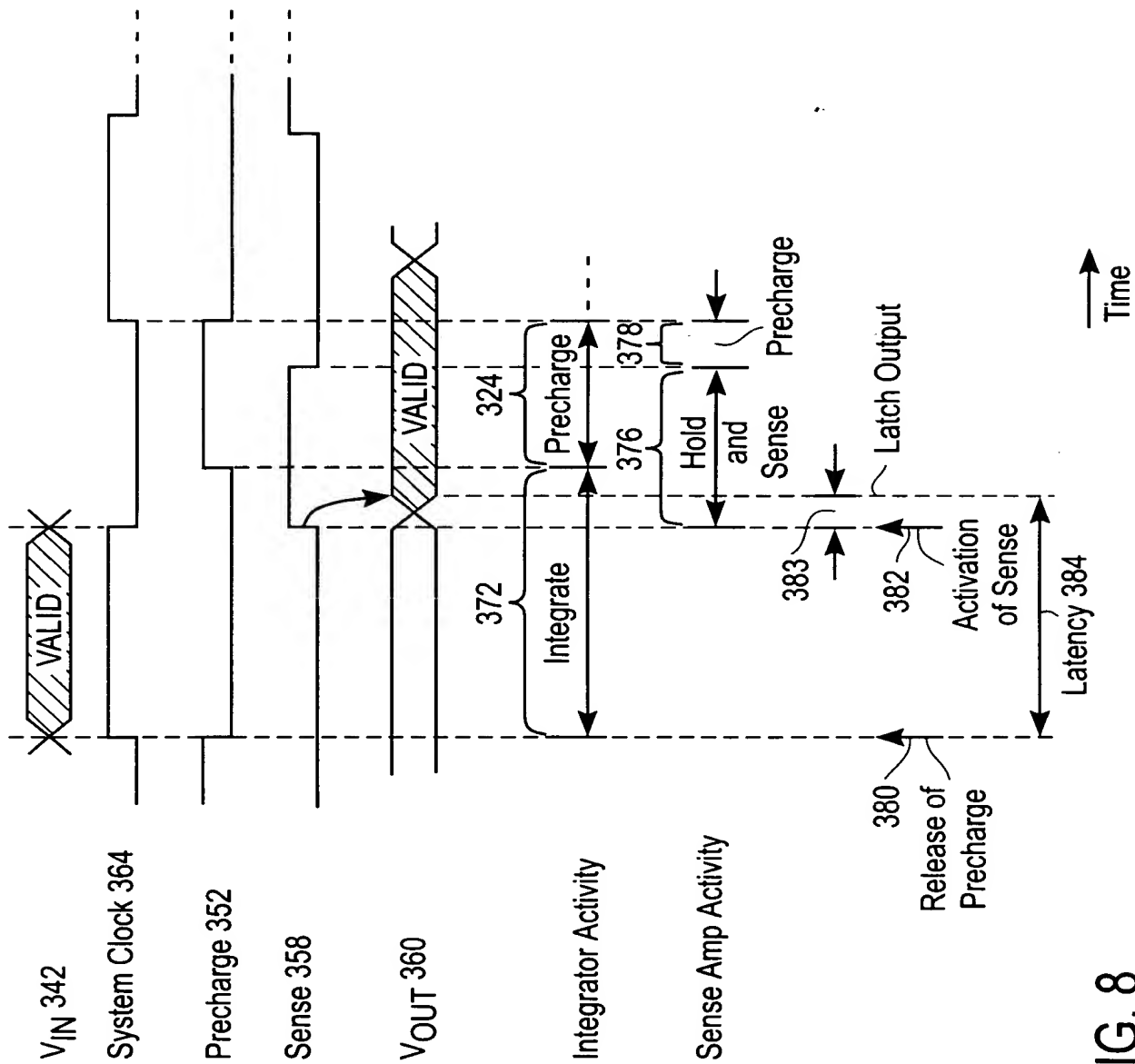


FIG. 8

390

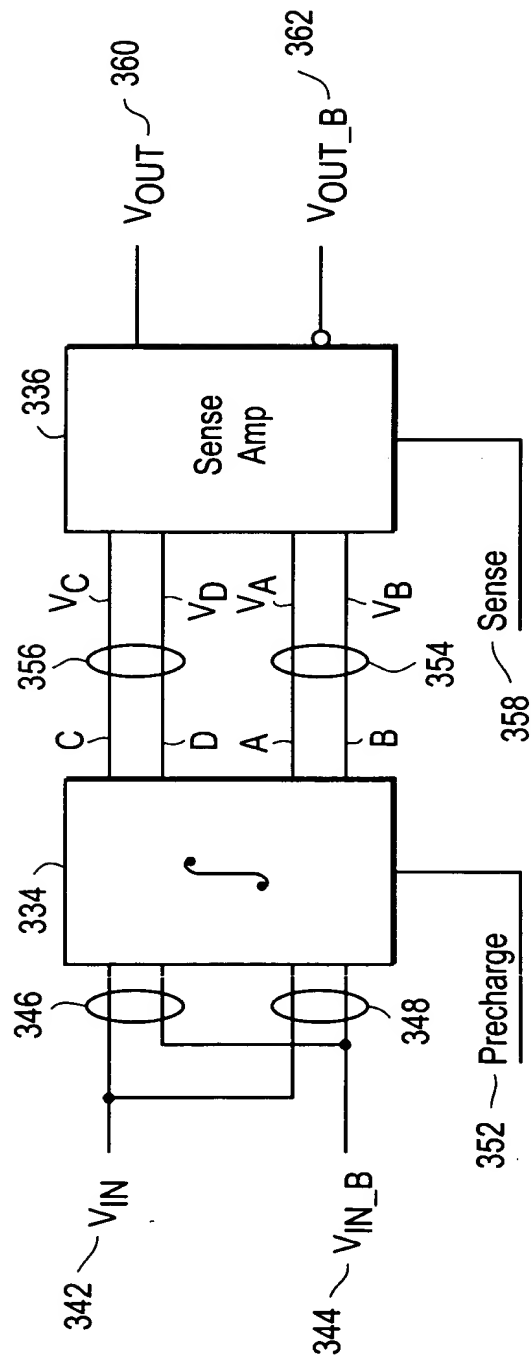


FIG. 9

Preamplifier  
332A

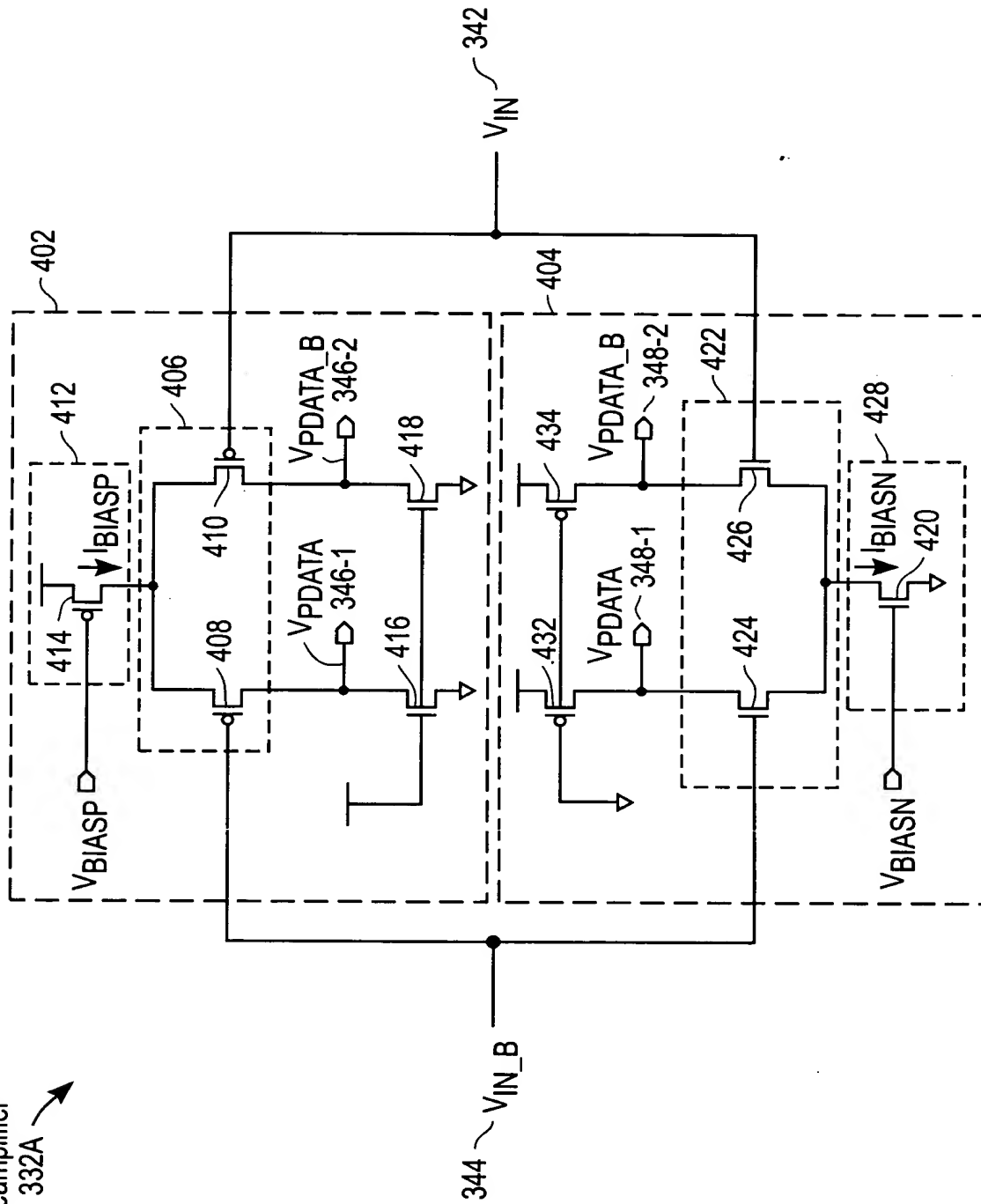


FIG. 10

334A

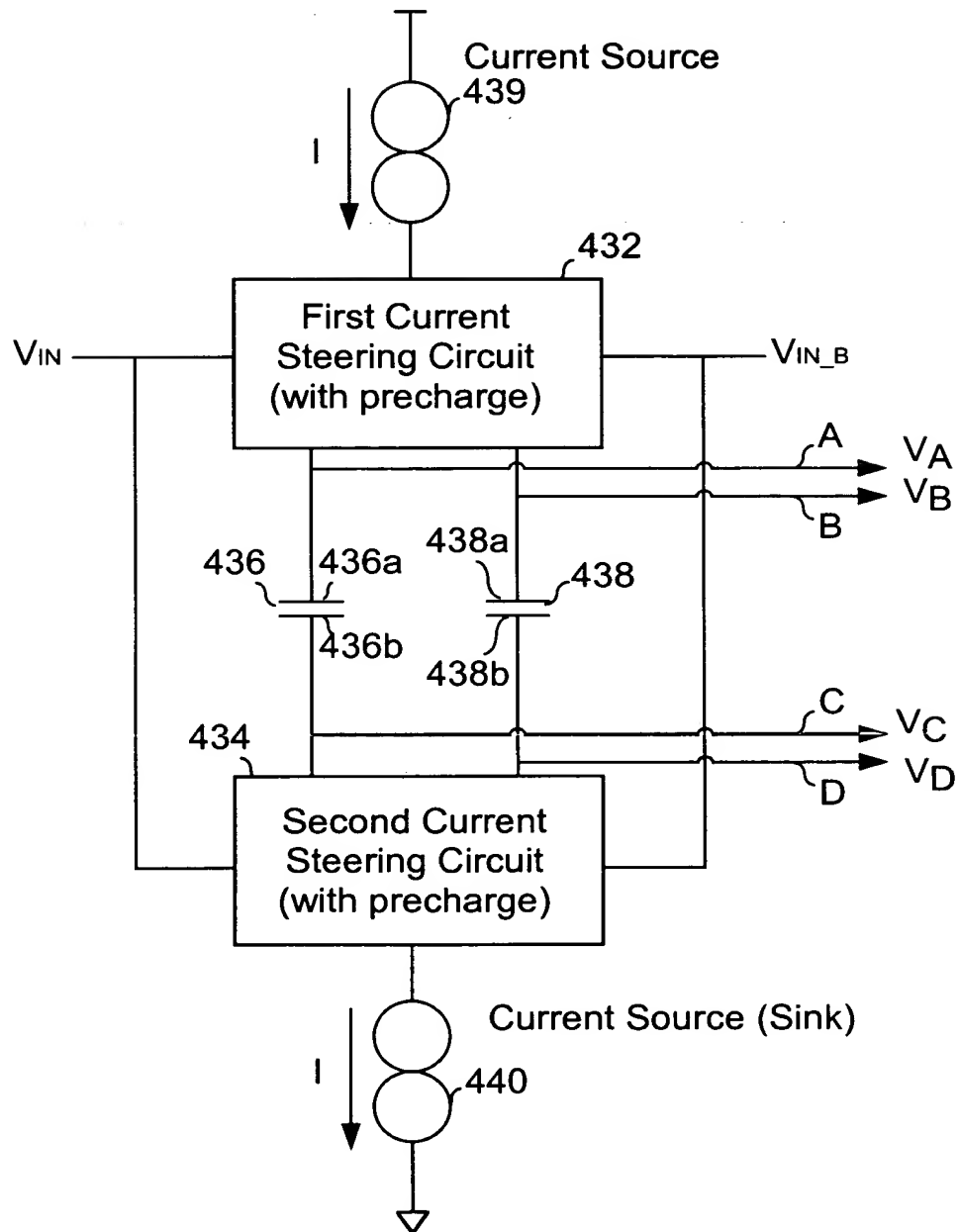


FIG. 11A

Integrator  
334B

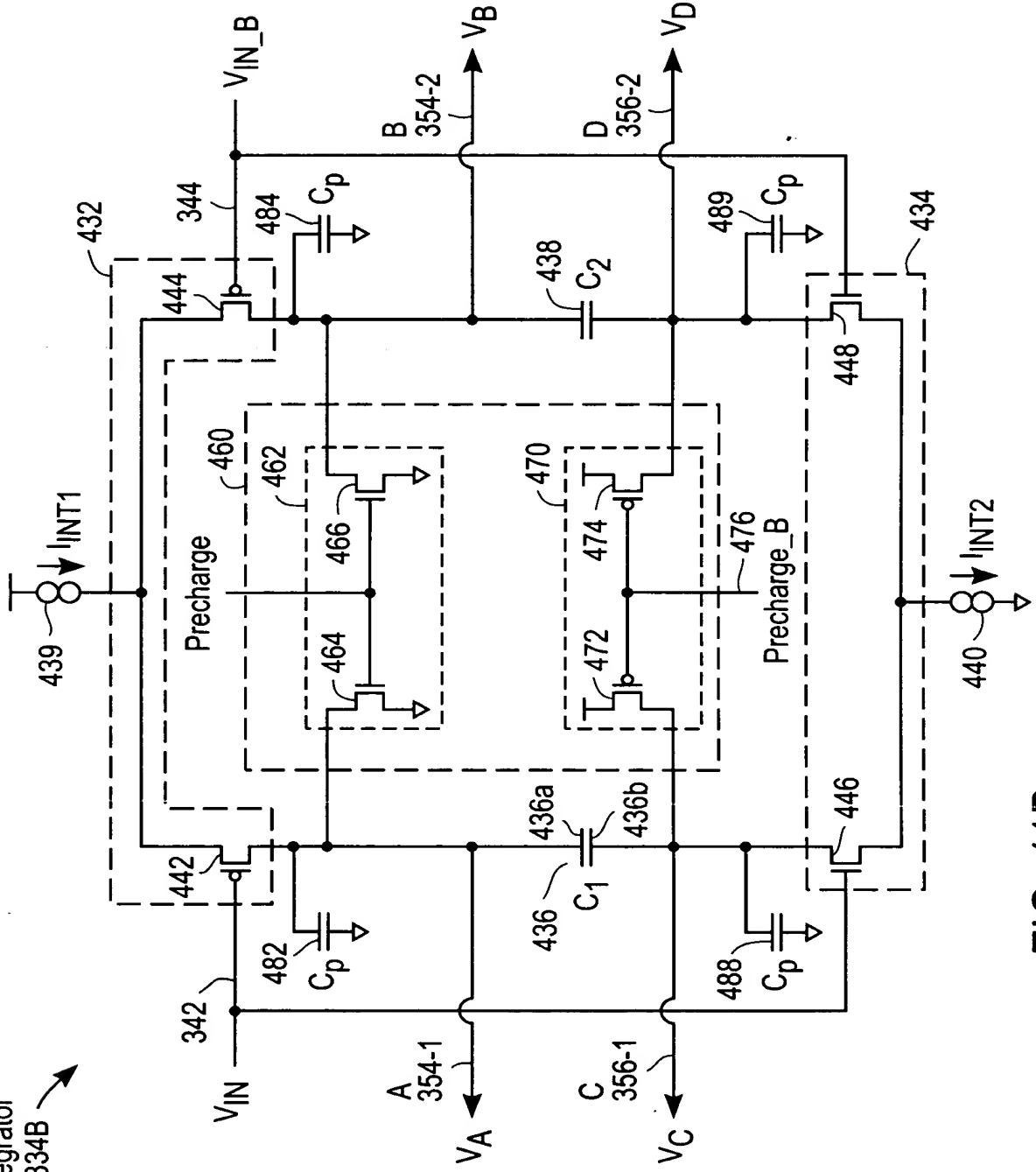


FIG. 11B

Integrator  
334C

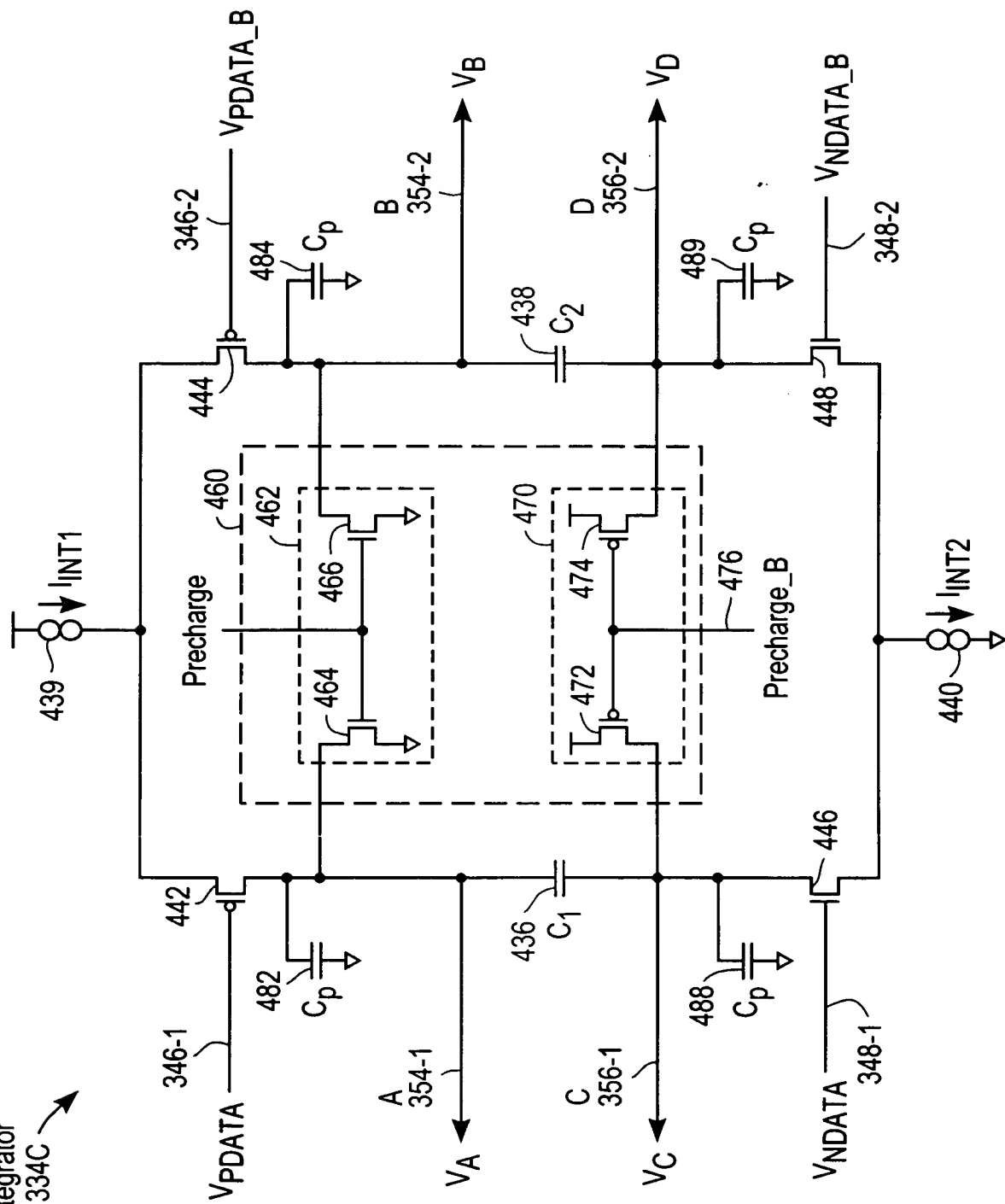


FIG. 11C

Integrator  
334D

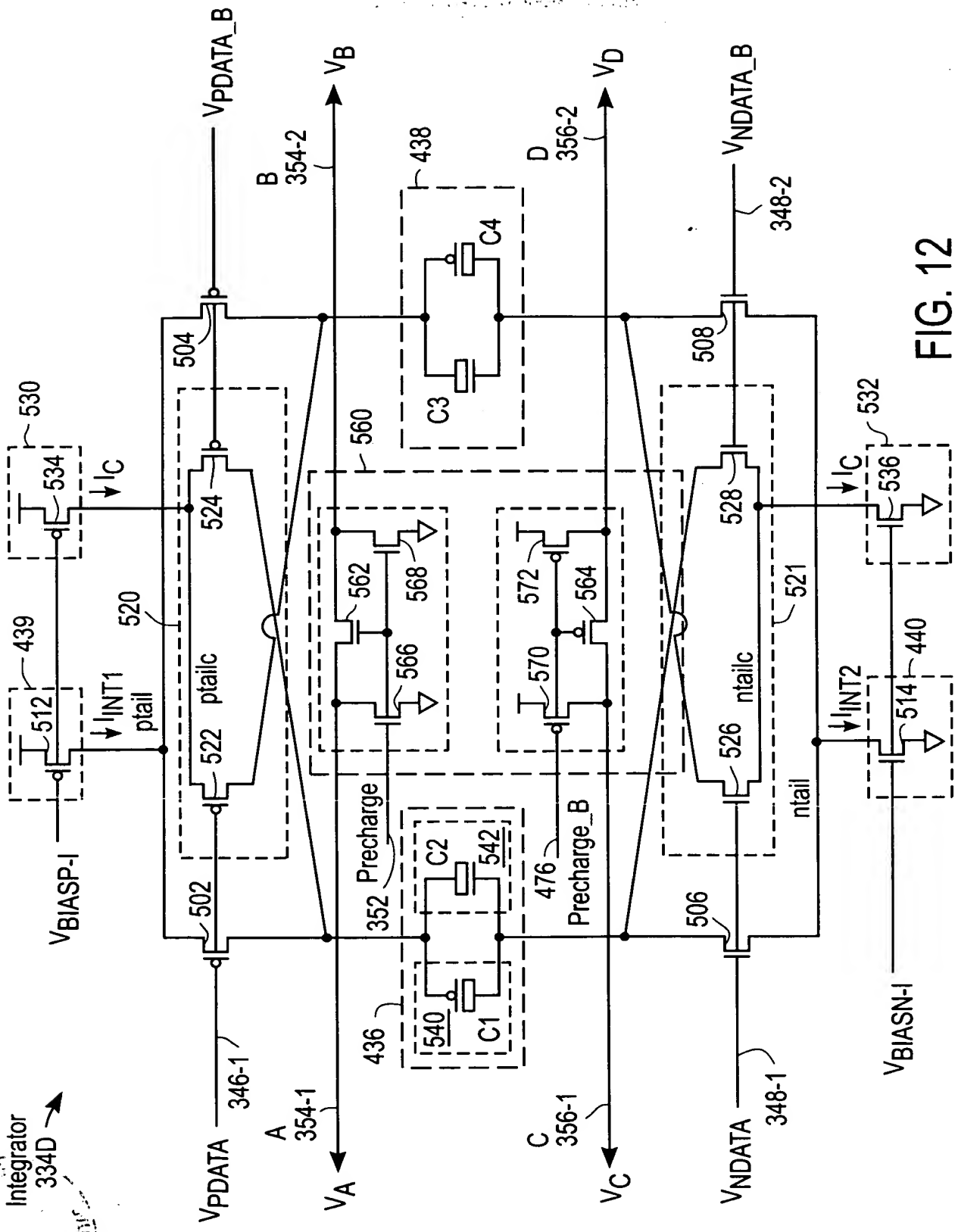


FIG. 12

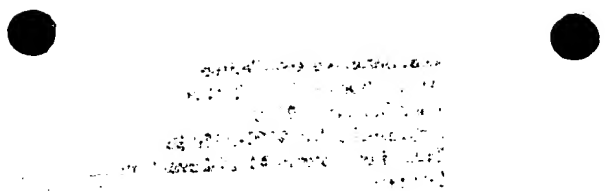
[illegible]

FIG. 13

Sense Amplifier and Latch

336E

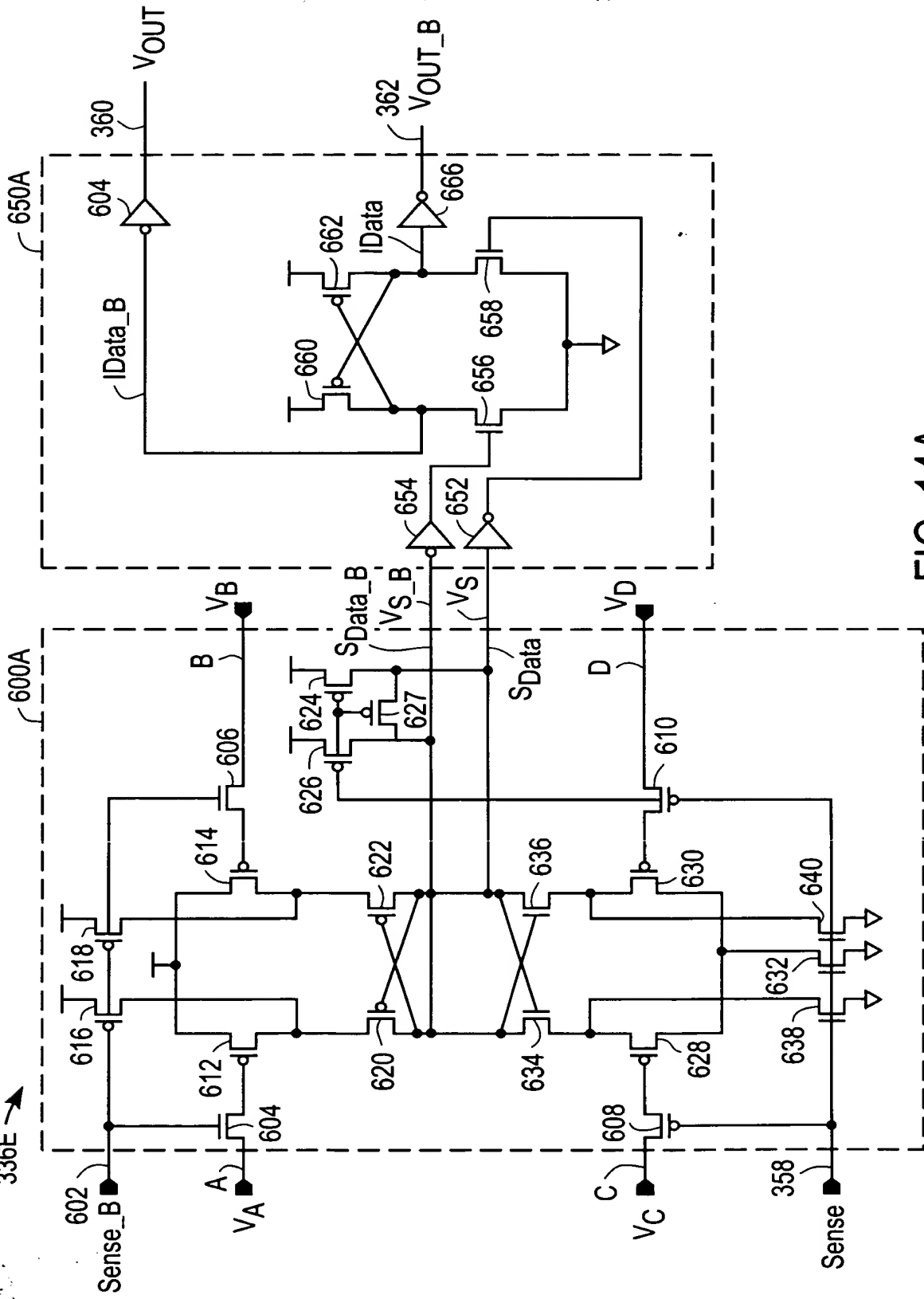


FIG. 14A

Sense Amplifier and Latch

336B

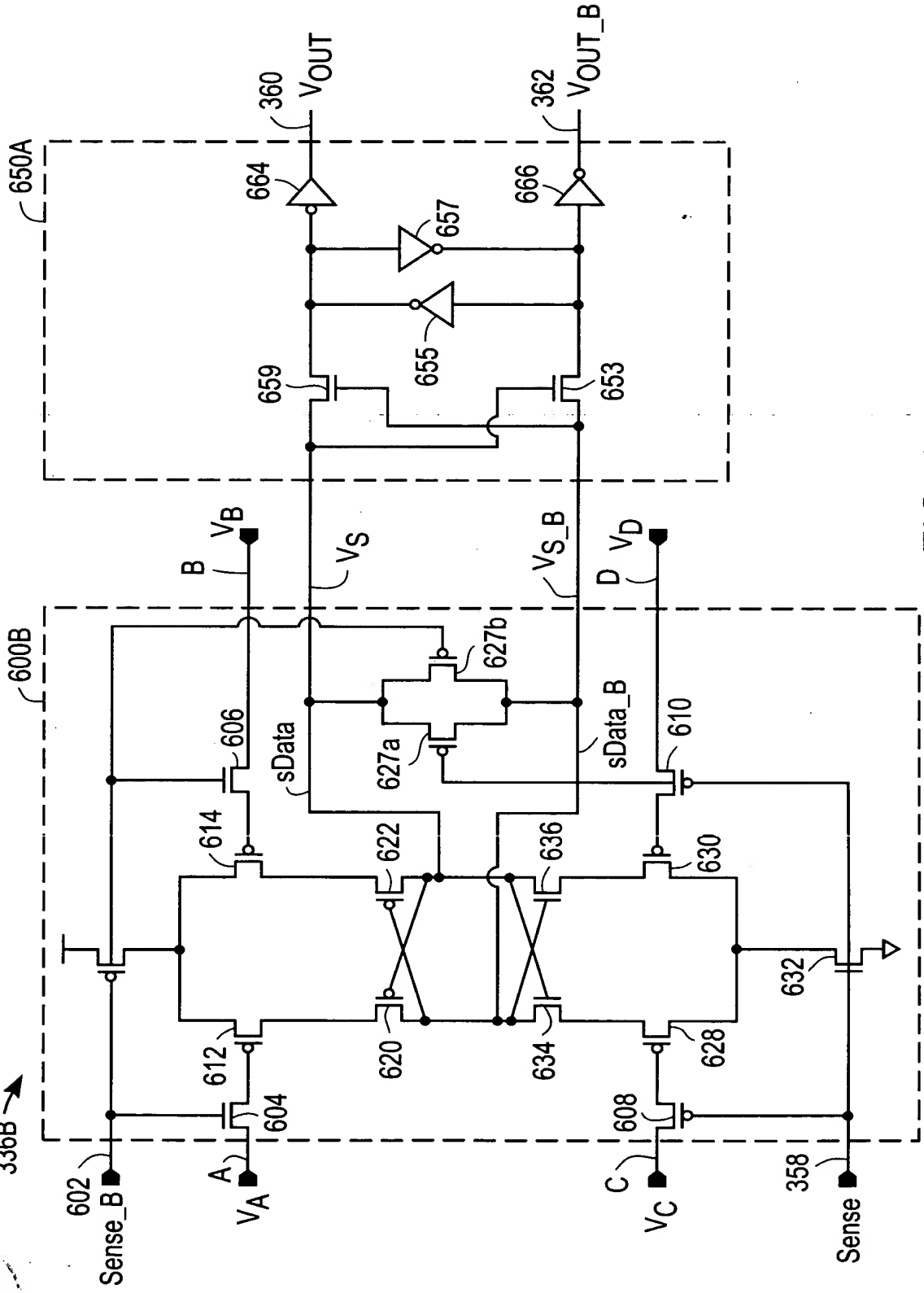
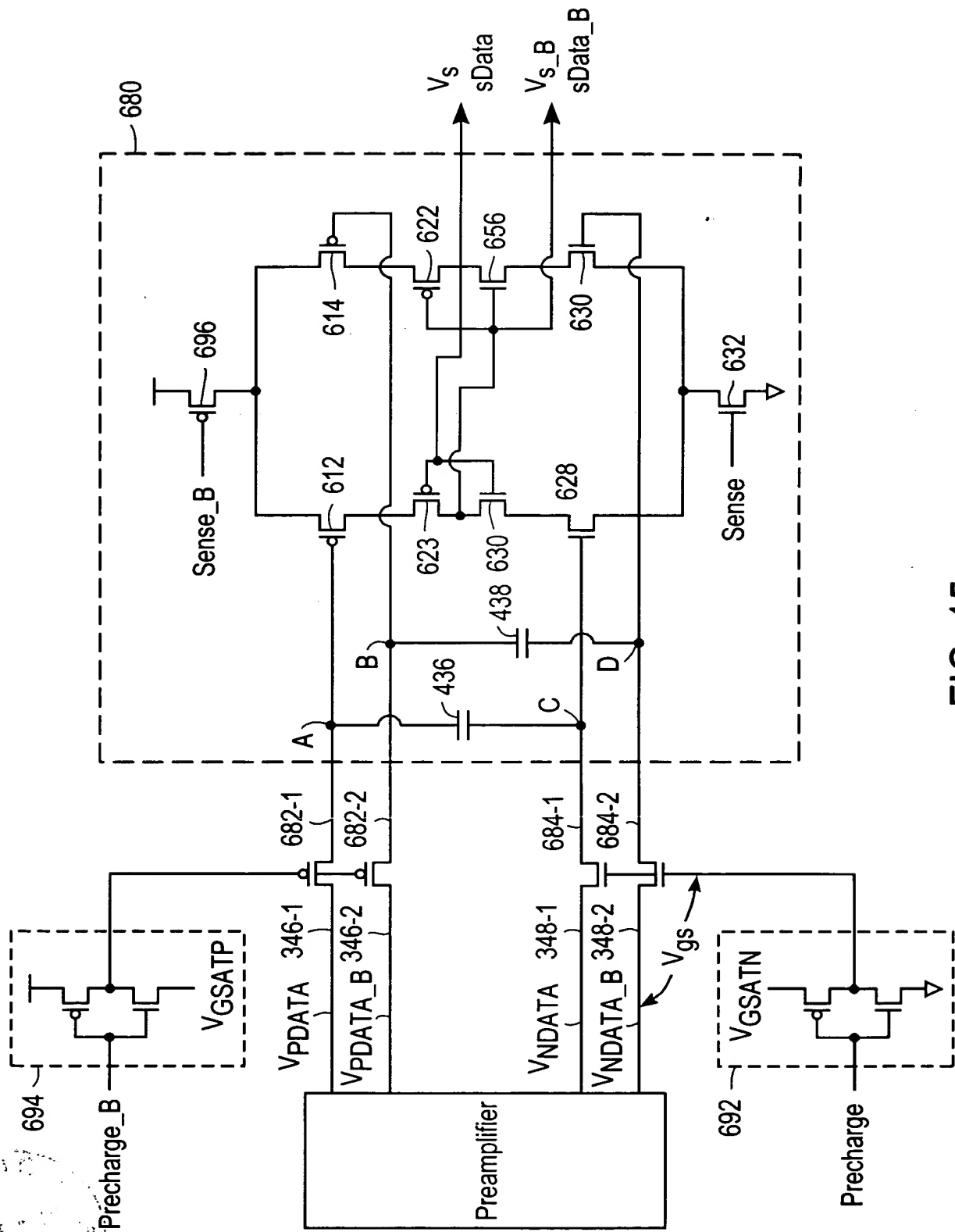


FIG. 14B



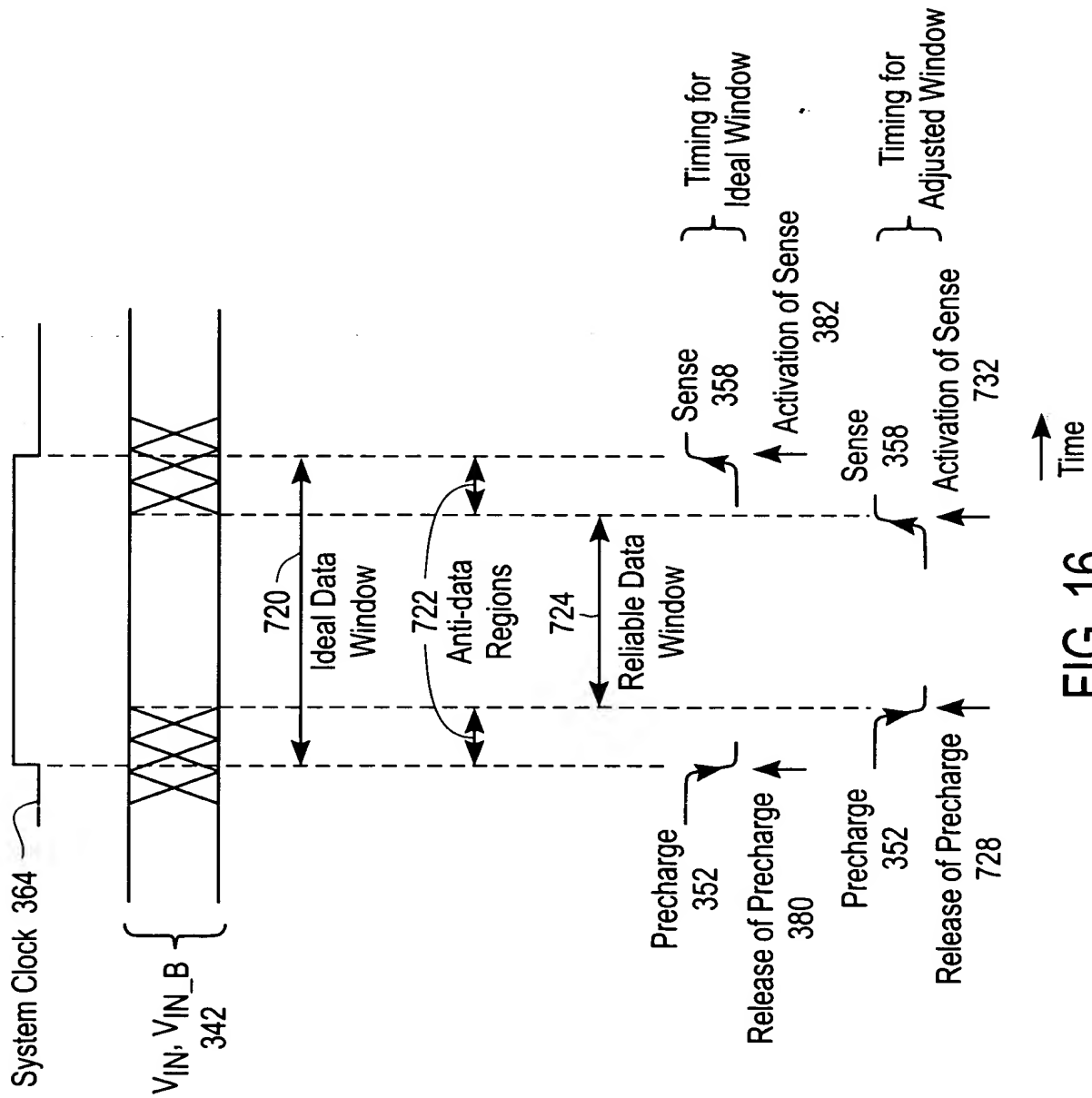
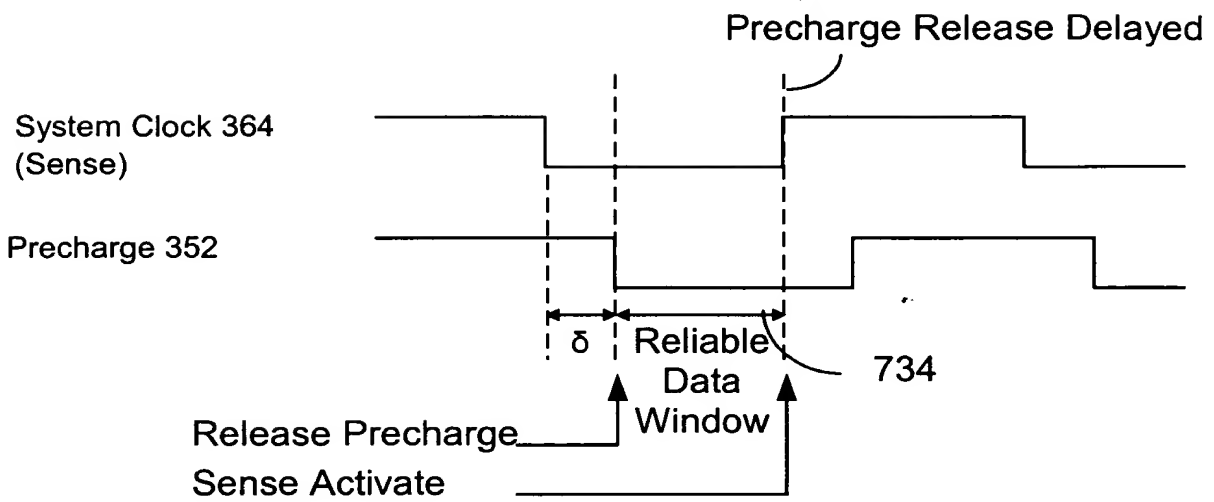
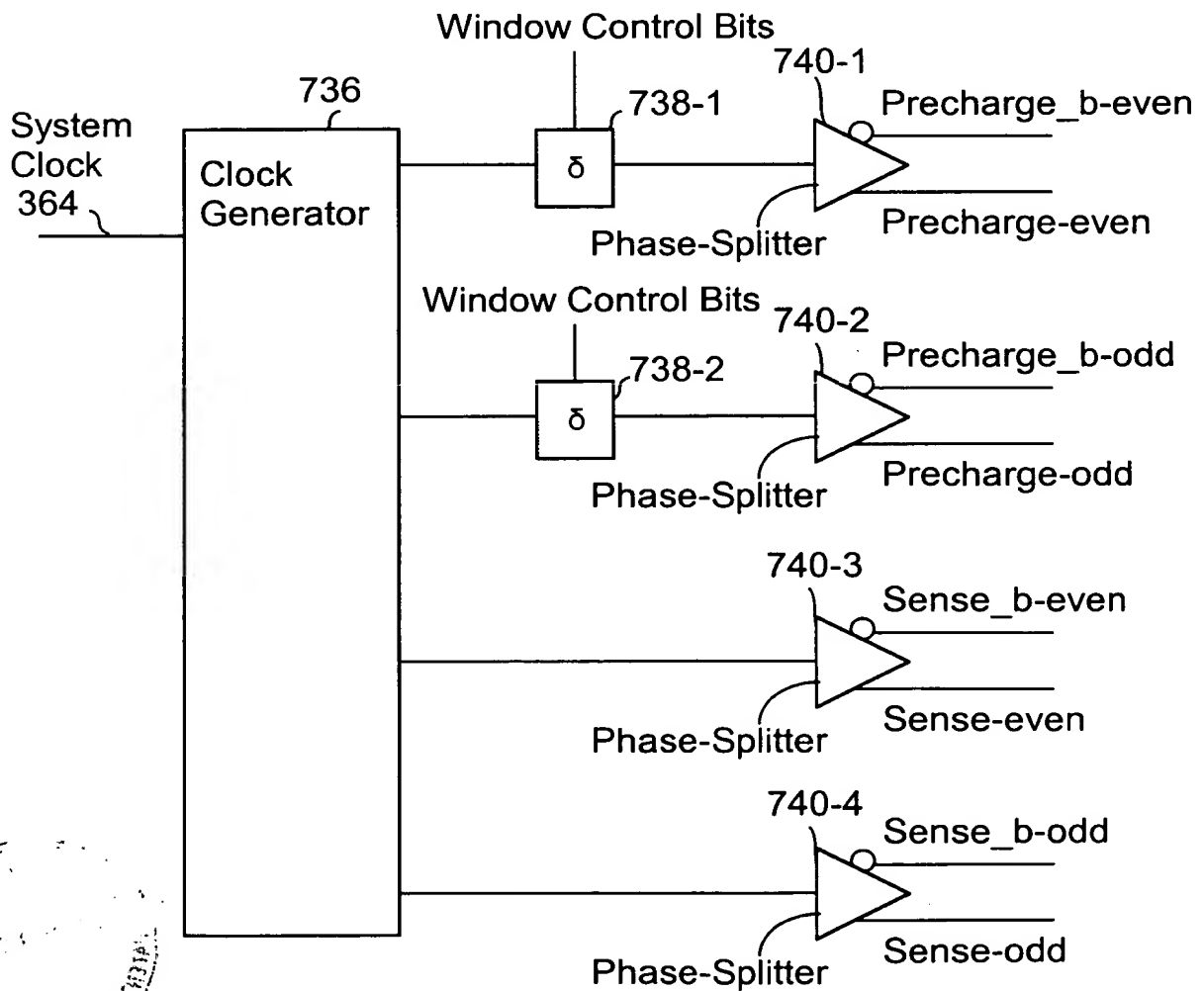


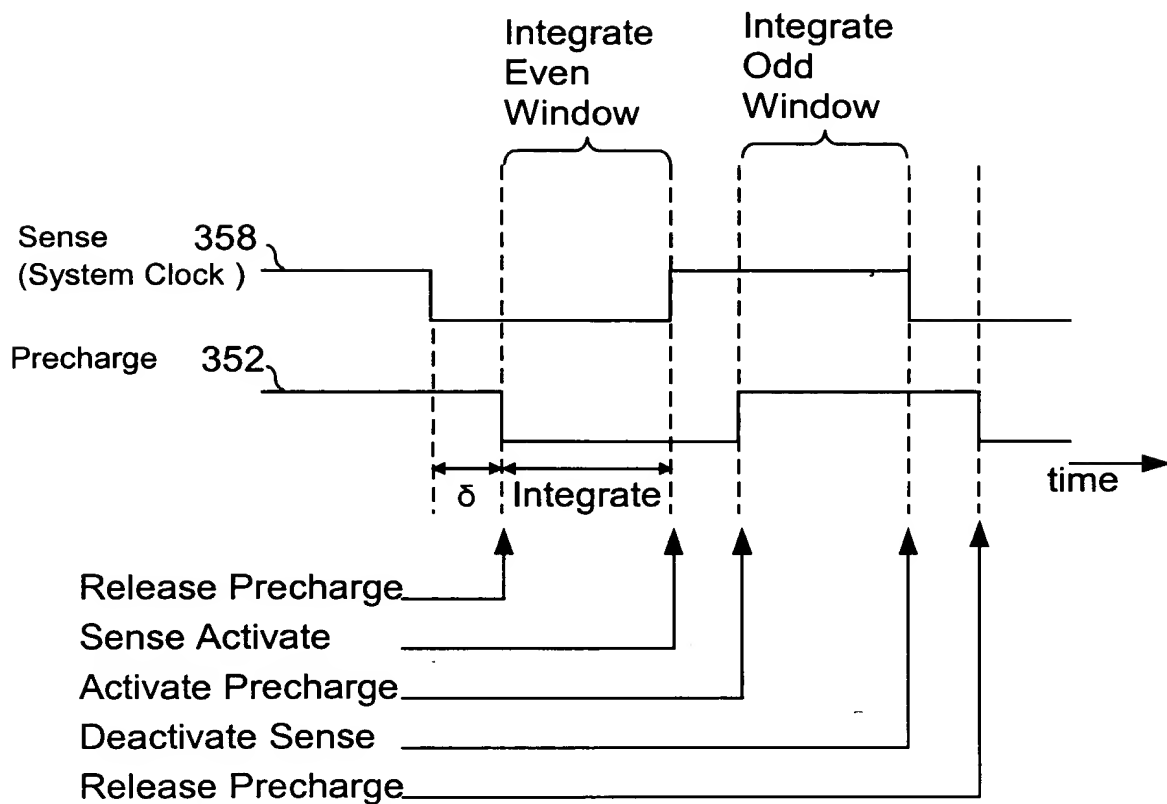
FIG. 16



**FIG. 17A**

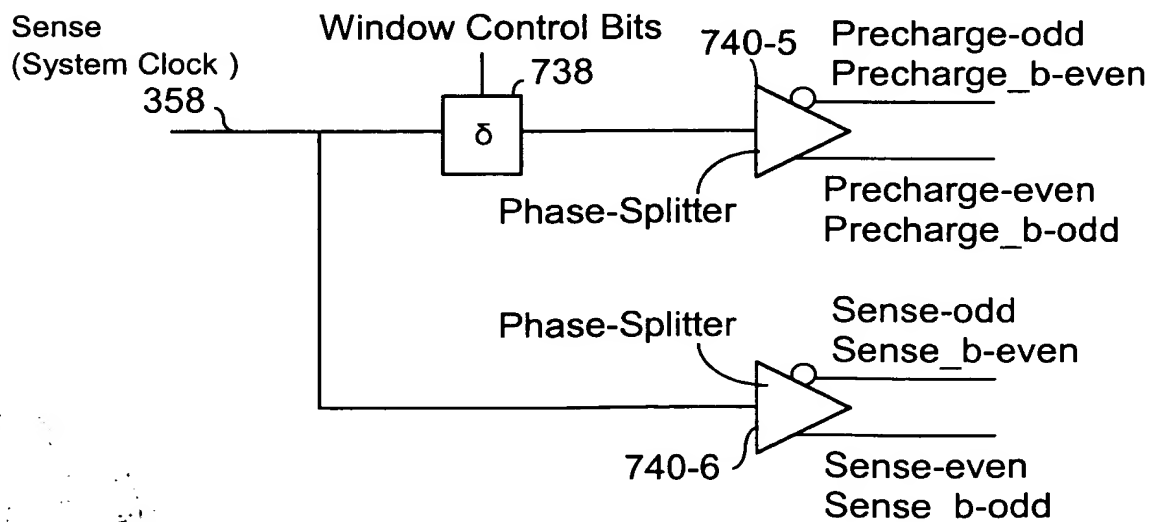


**FIG. 17B**



Timing Diagram of Precharge and Sense Signals

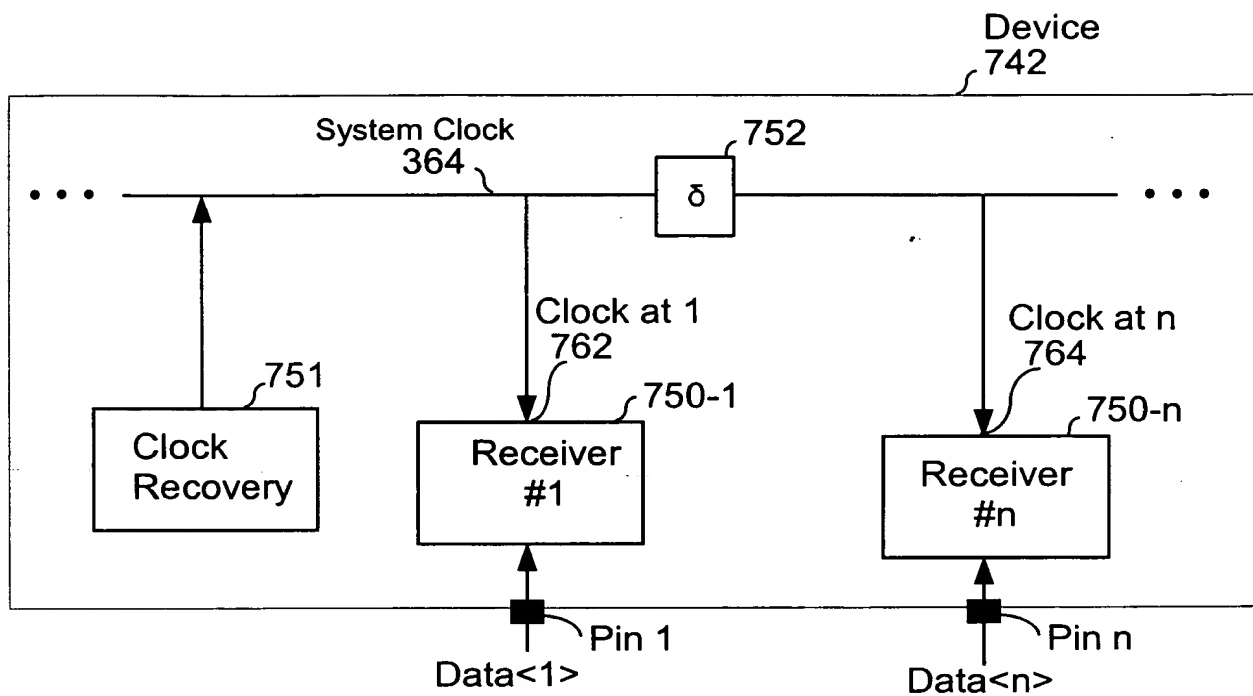
**FIG. 17C**



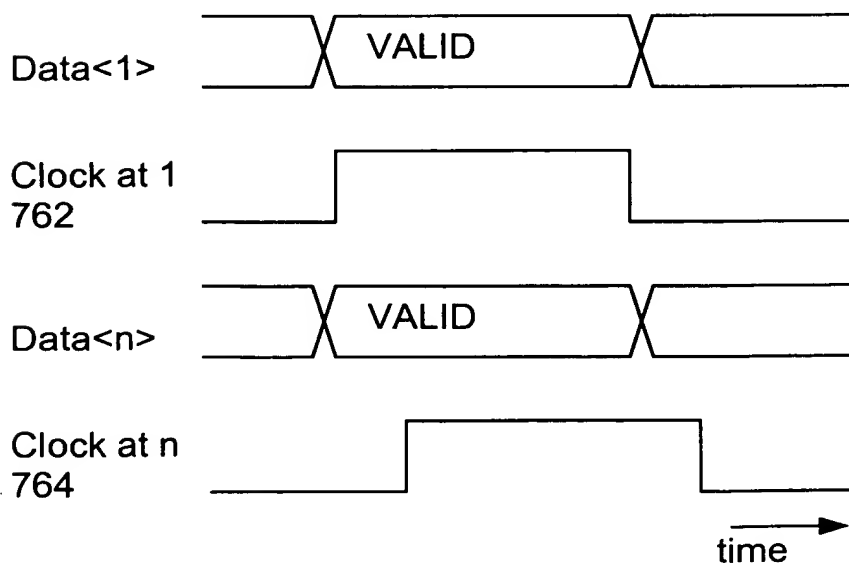
Circuit for Timing Diagram of Fig.17C

**FIG. 17D**

1. A system for receiving data from a plurality of devices, comprising:  
 a. a system clock;  
 b. a plurality of receivers, each receiver receiving data from a device and receiving the system clock;  
 c. a clock recovery circuit receiving the system clock and outputting a clock signal to each receiver.



**FIG. 18**



**FIG. 19**



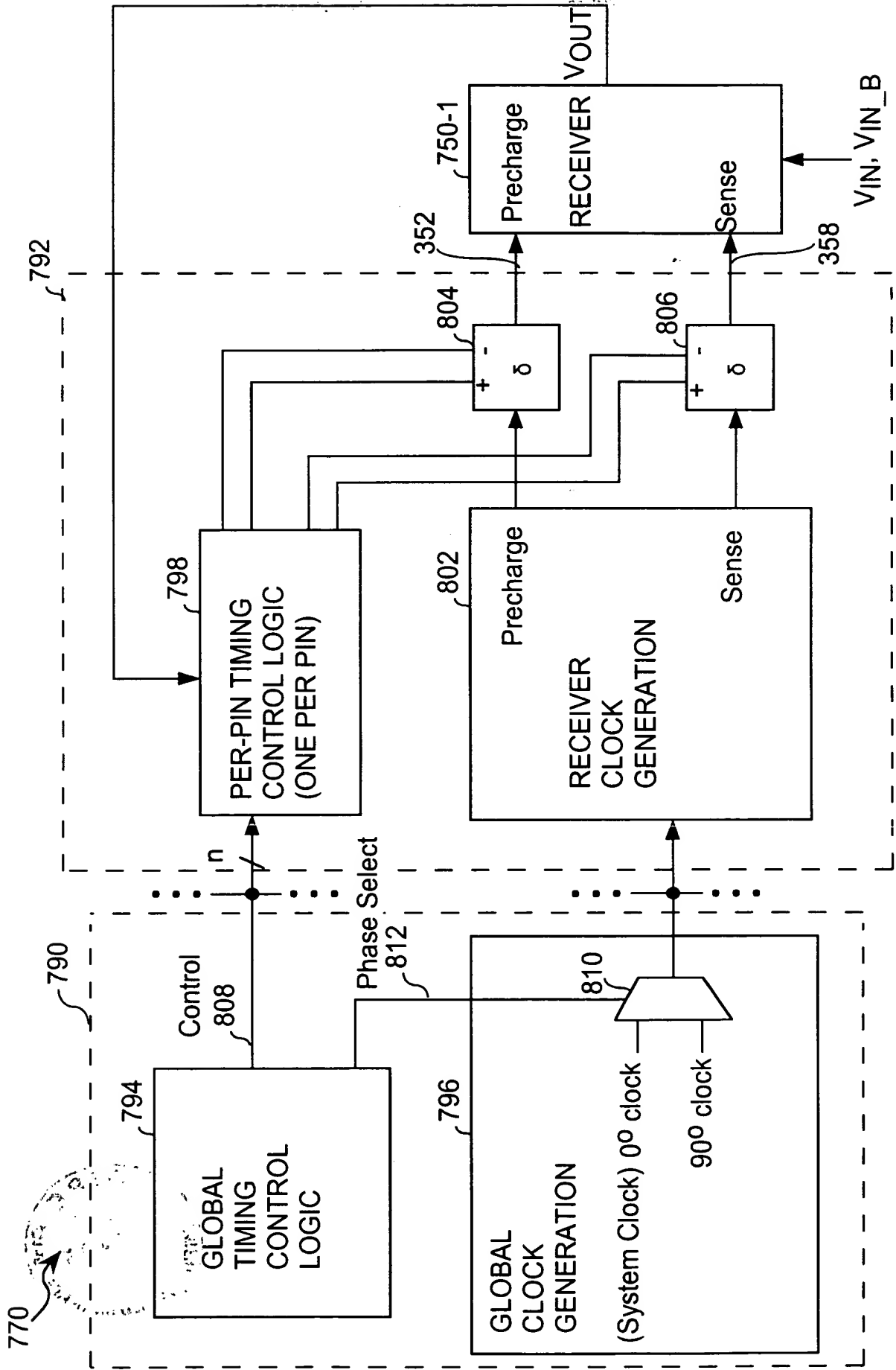
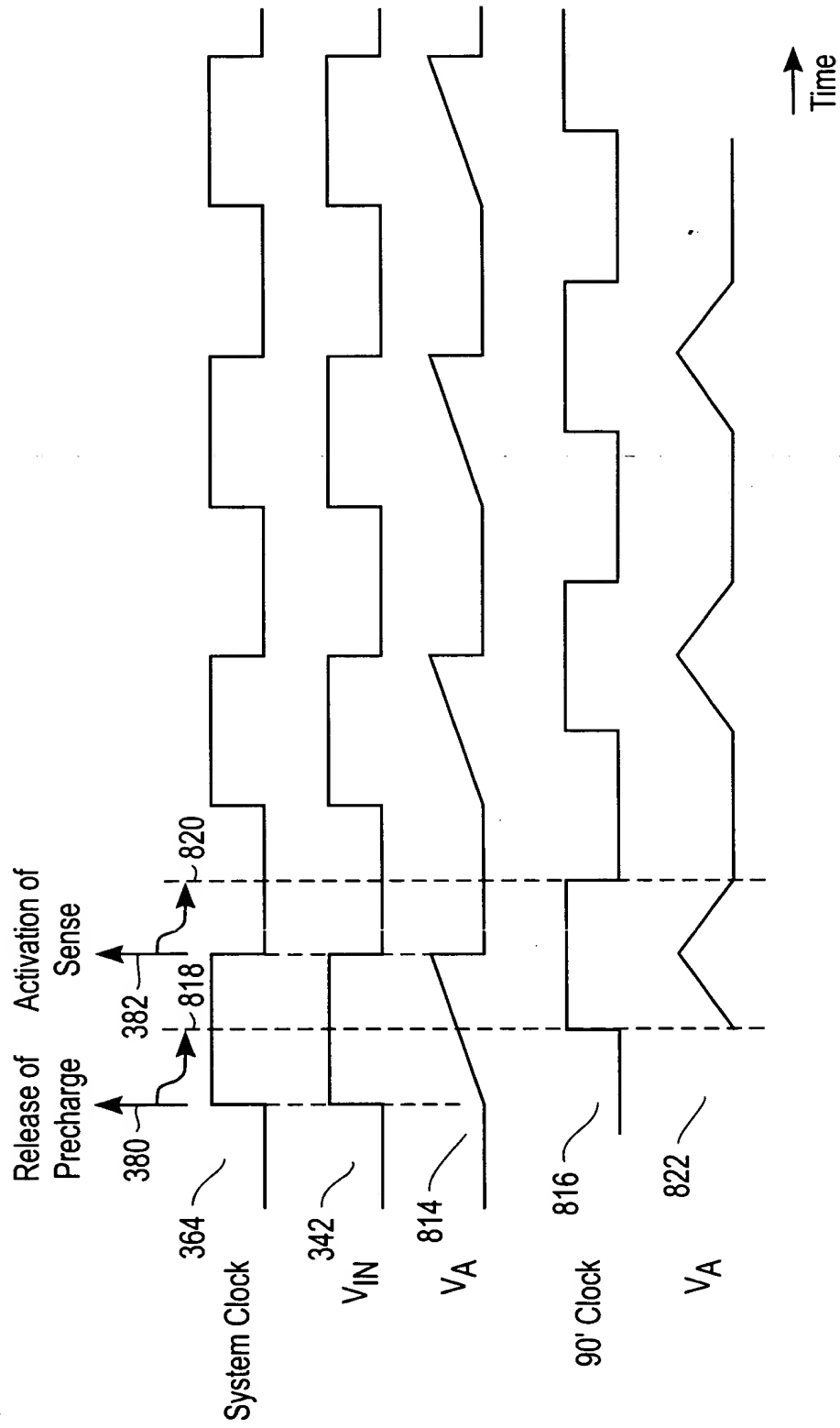


FIG. 20



804 →

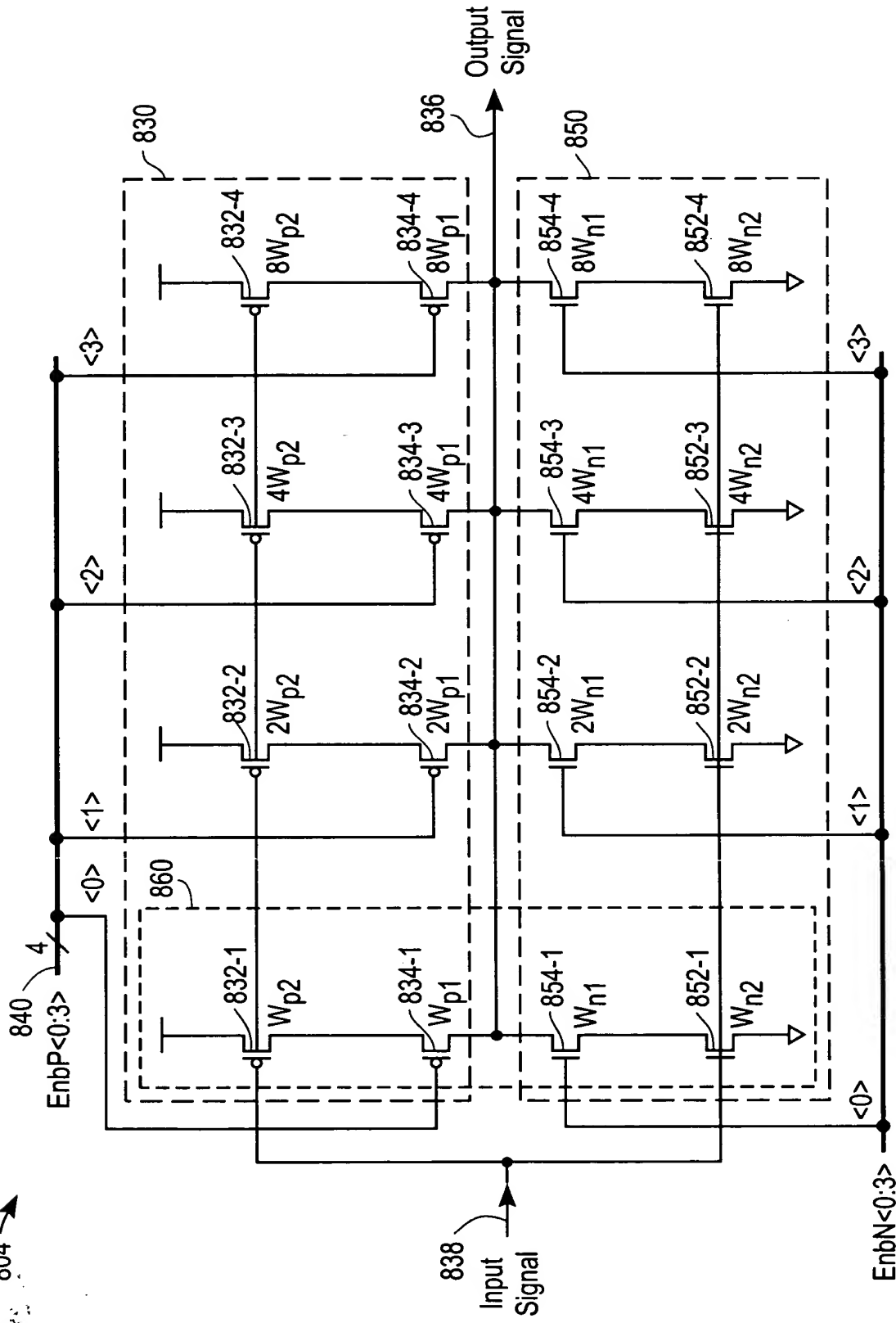


FIG. 22

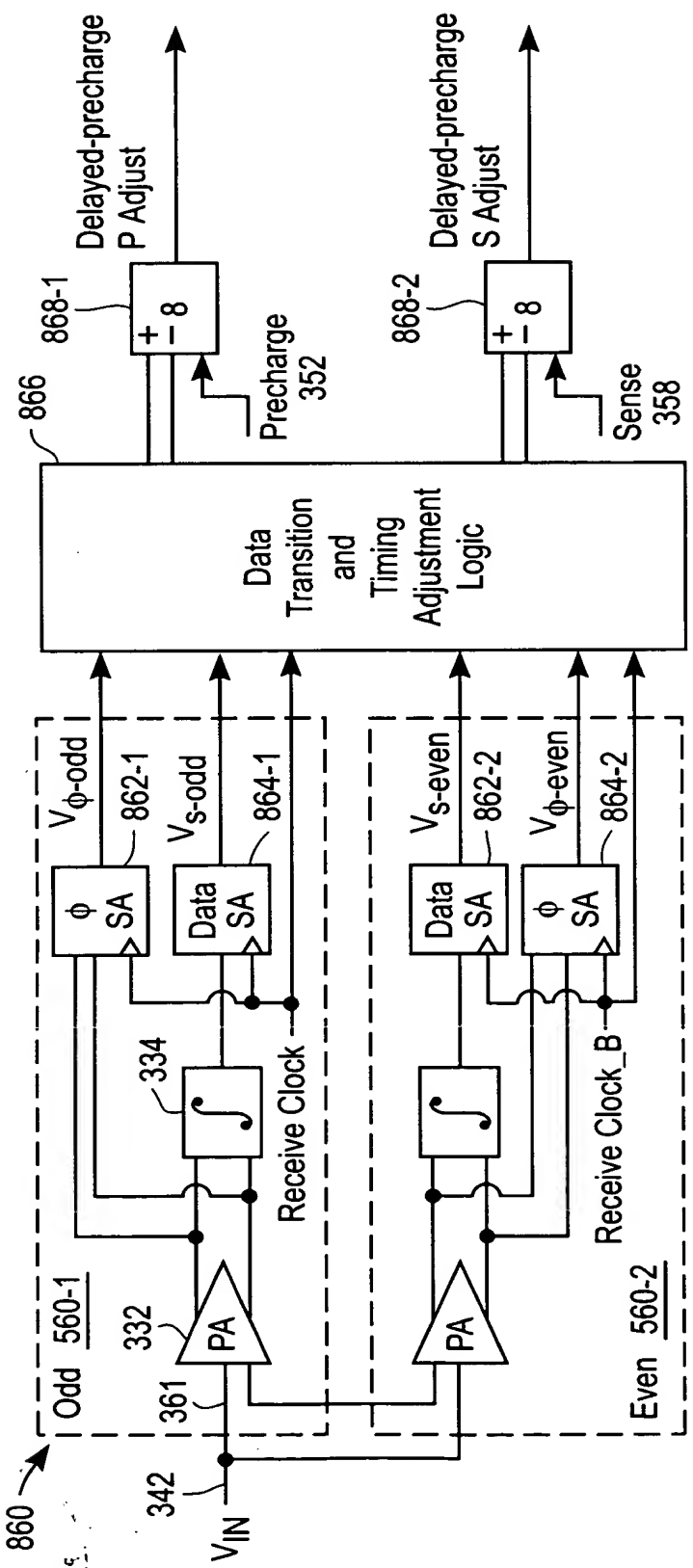


FIG. 23A

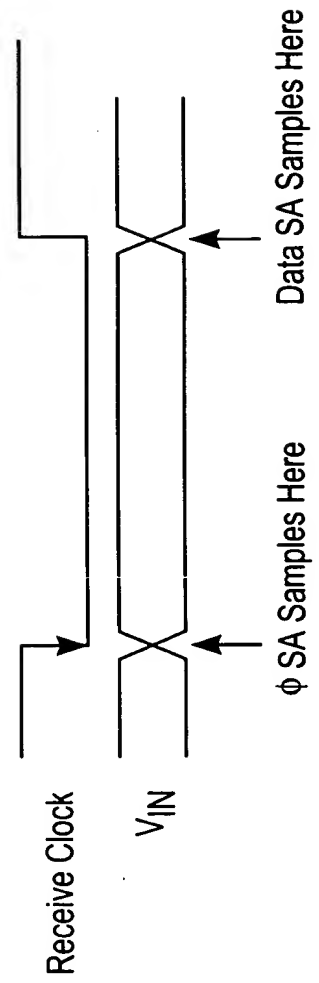


FIG. 23B

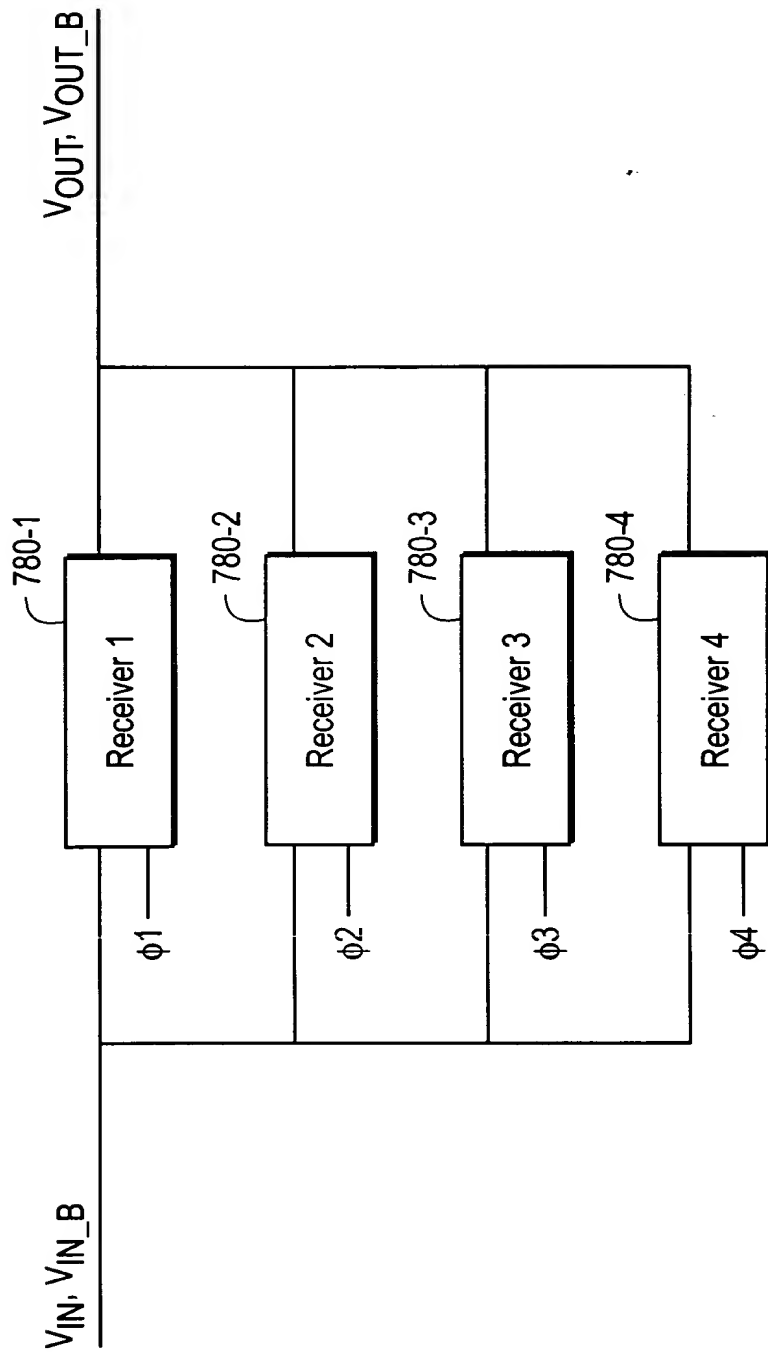


FIG. 24

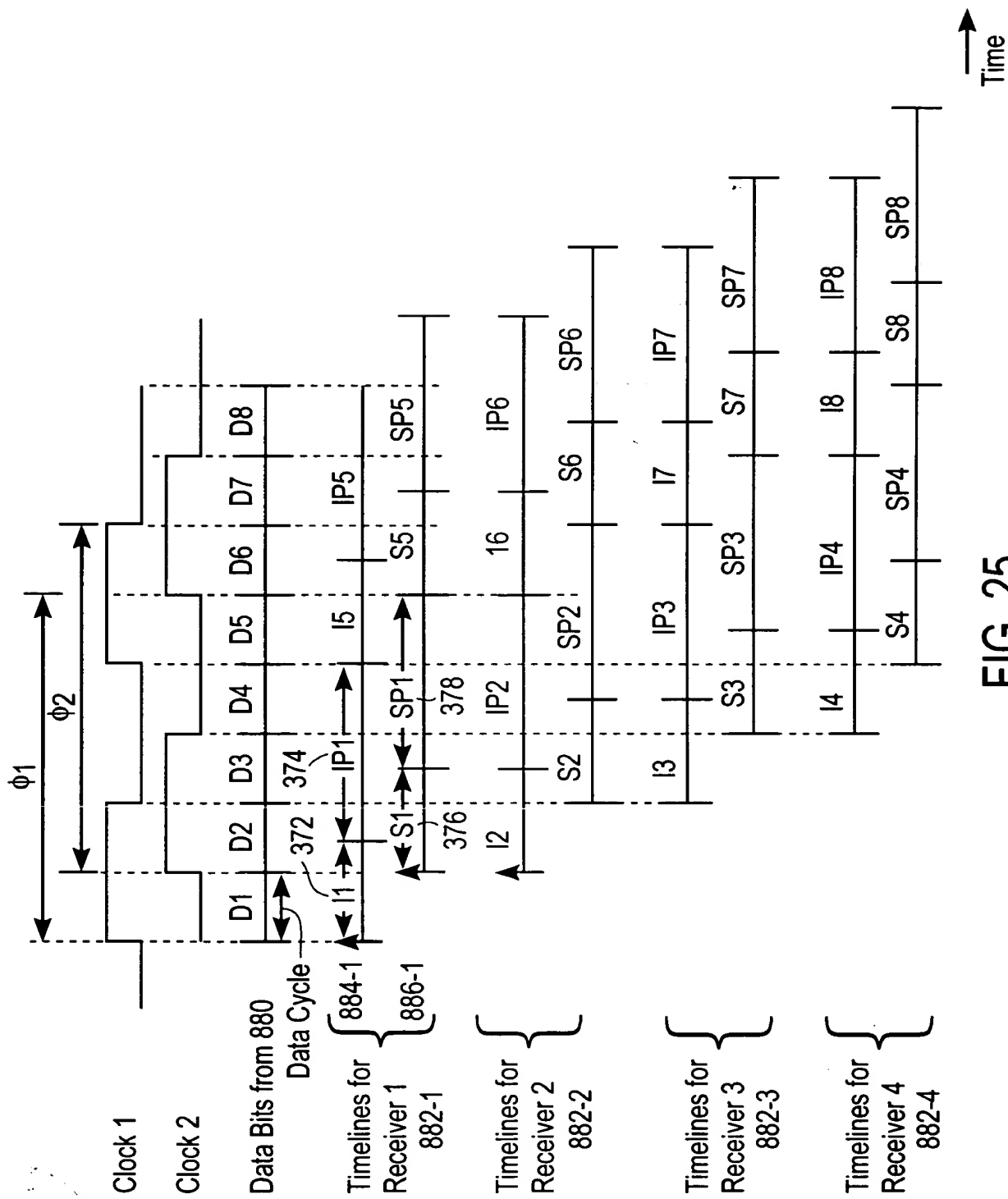


FIG. 25

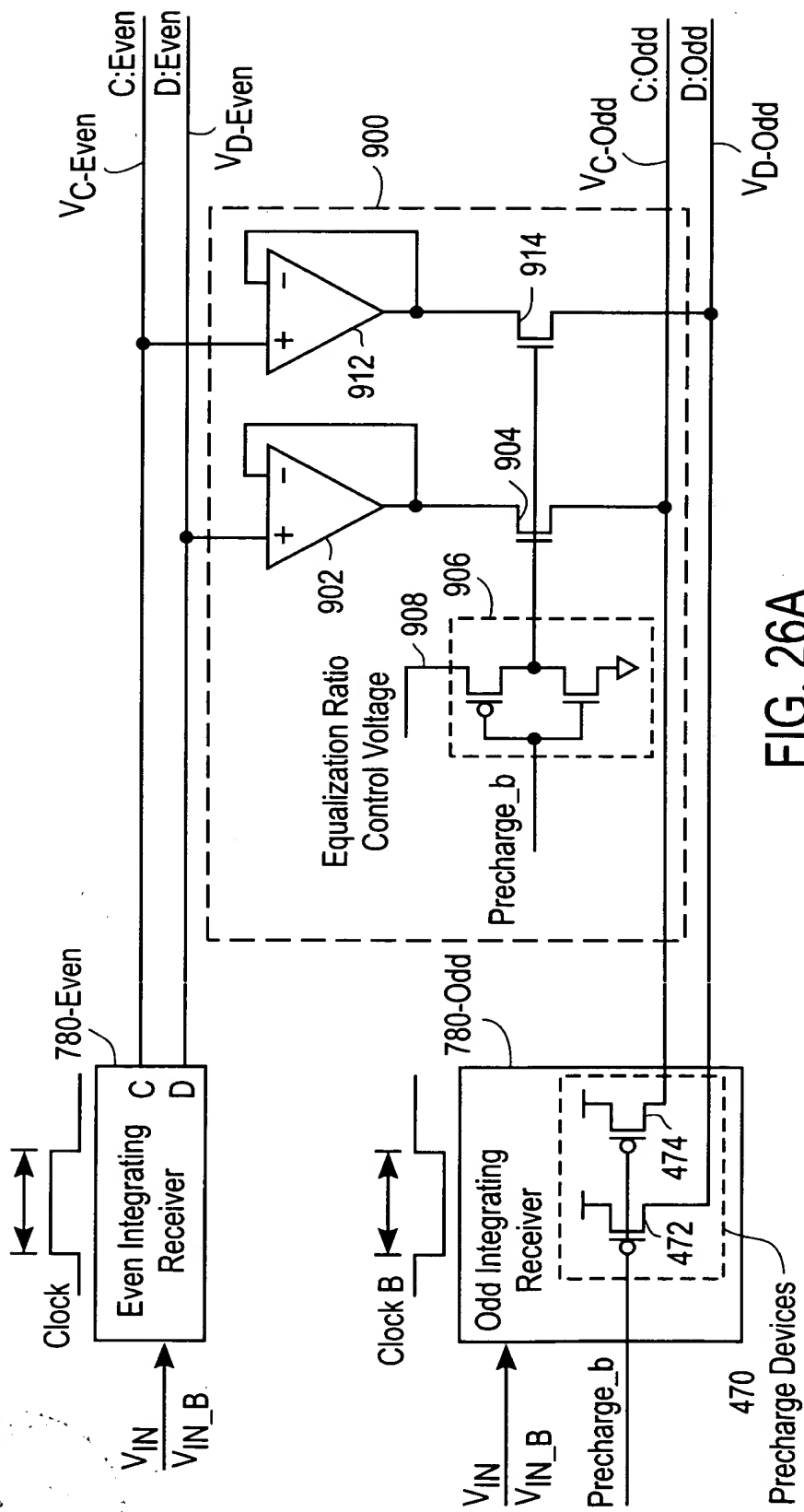


FIG. 26A

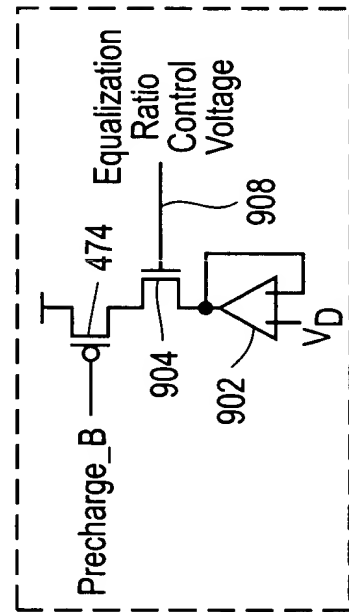


FIG. 26B

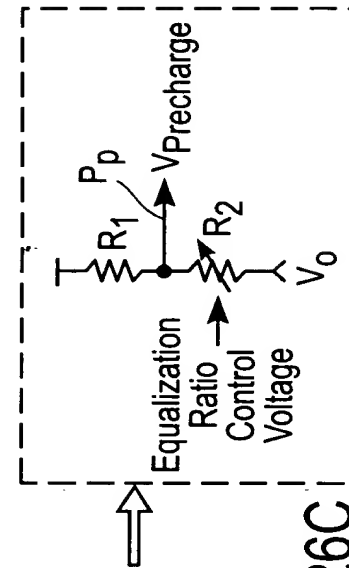


FIG. 26C

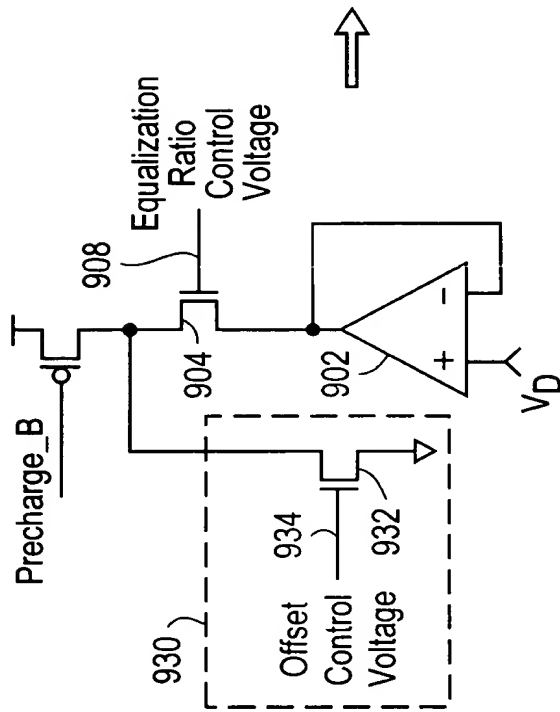


FIG. 27A

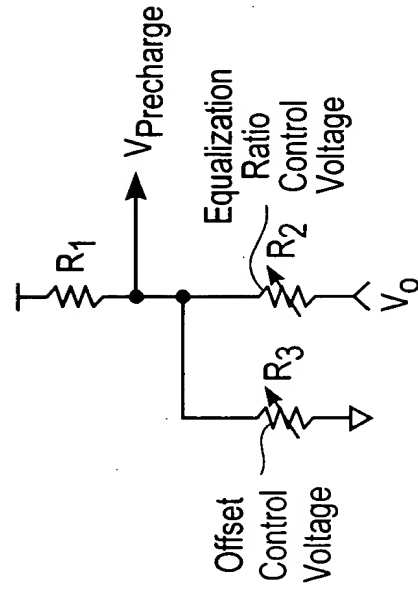


FIG. 27B

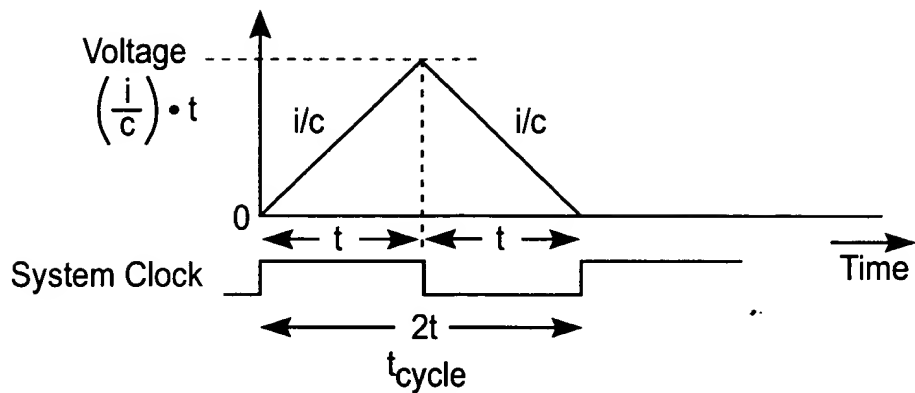


FIG. 28A

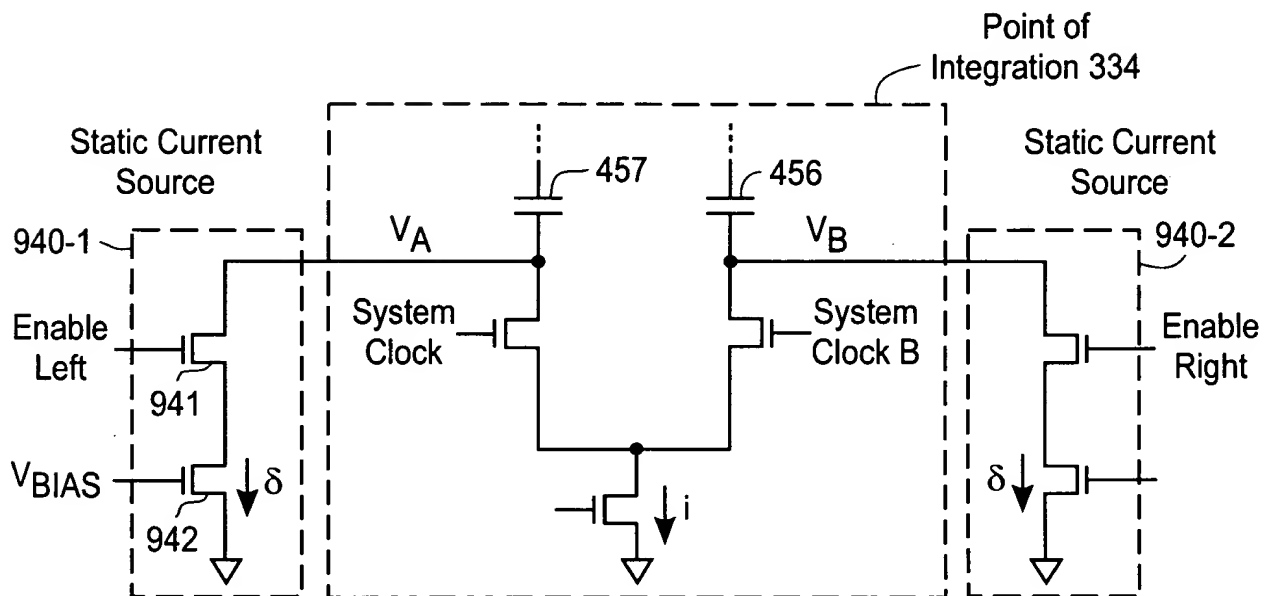


FIG. 28B

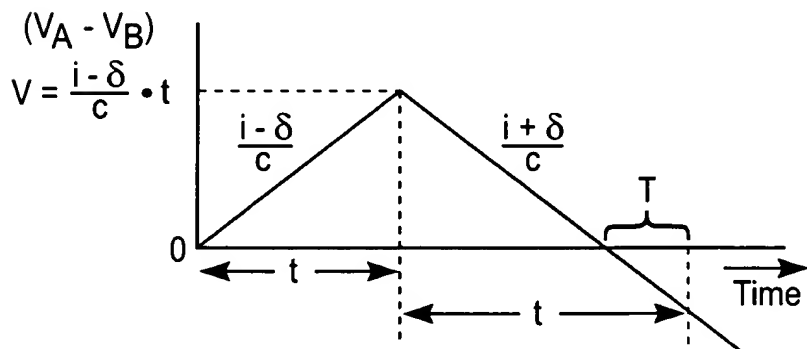


FIG. 28C

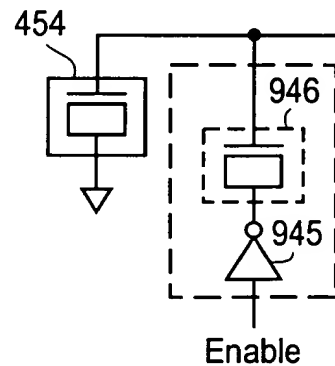
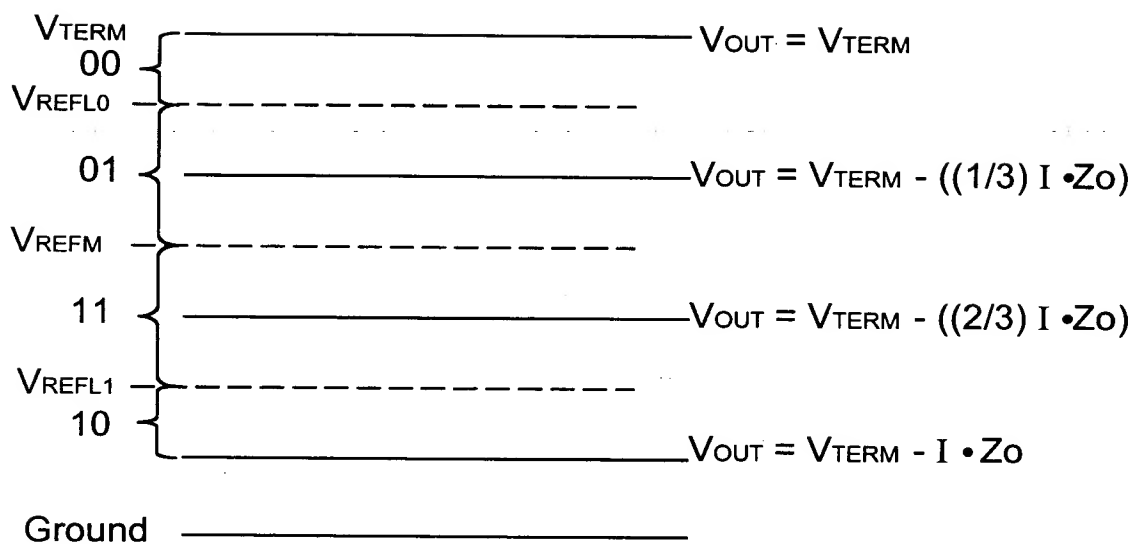
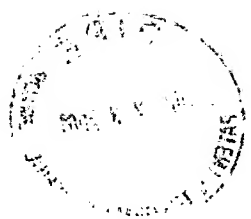
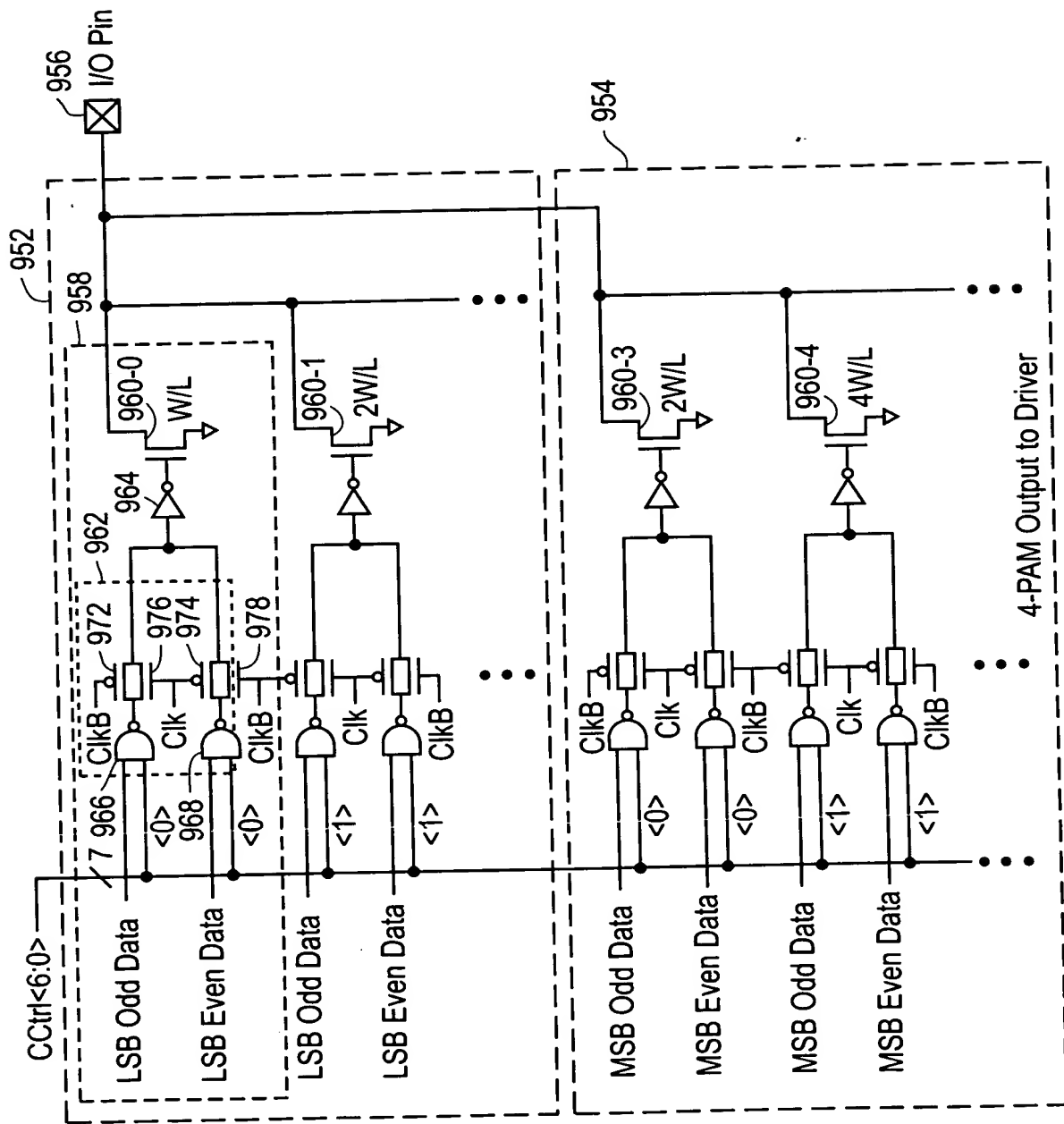


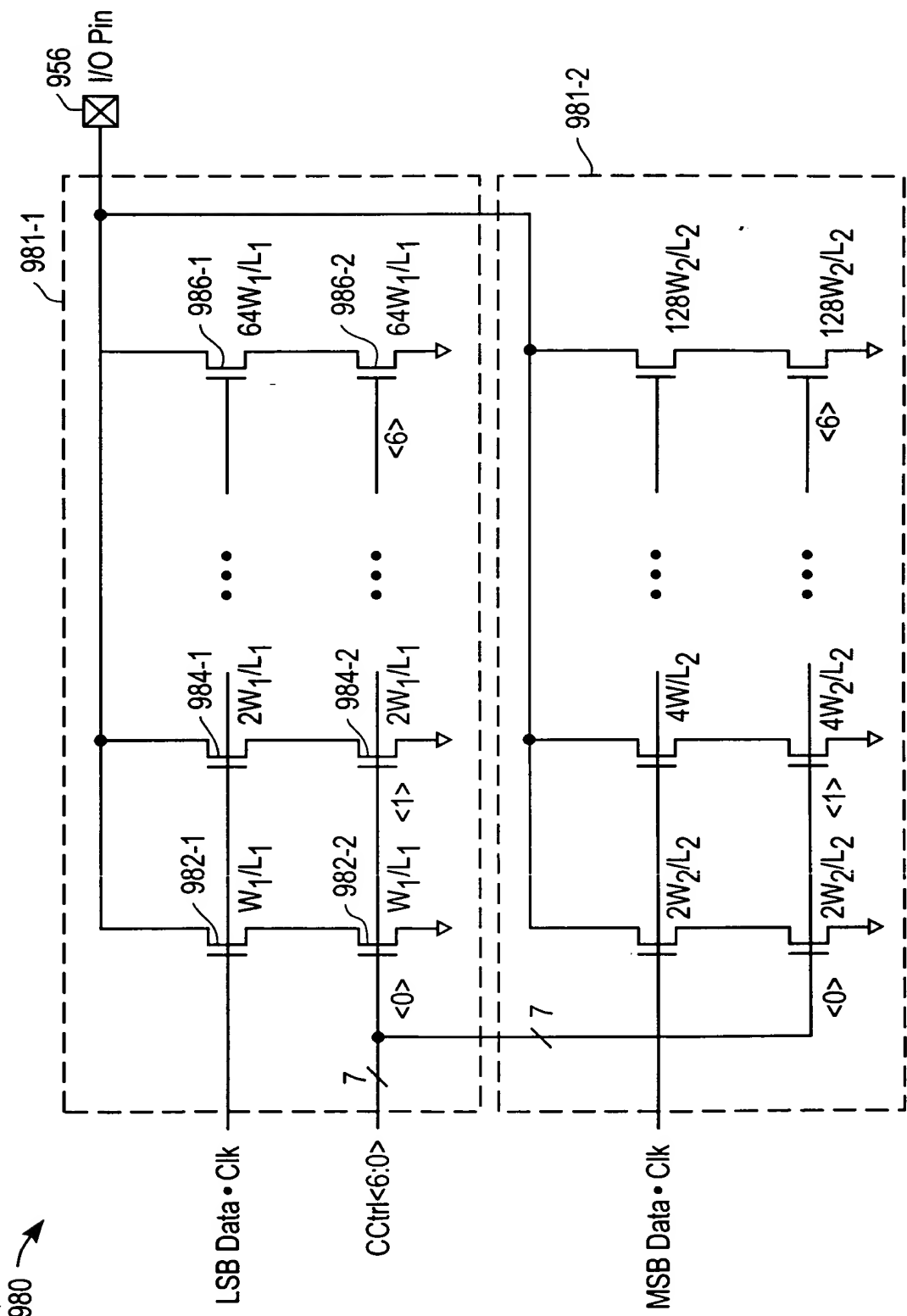
FIG. 28D



**FIG. 29**







4-PAM Output Driver

FIG. 31

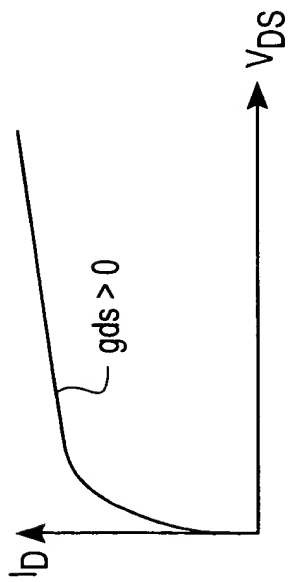
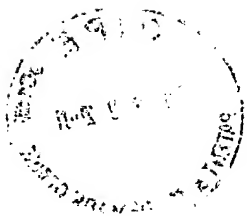


FIG. 32A

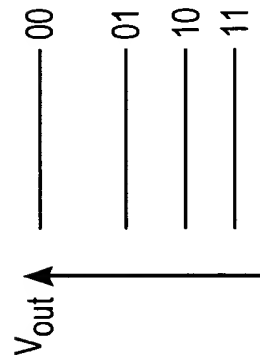


FIG. 32B

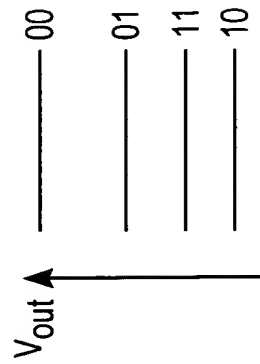
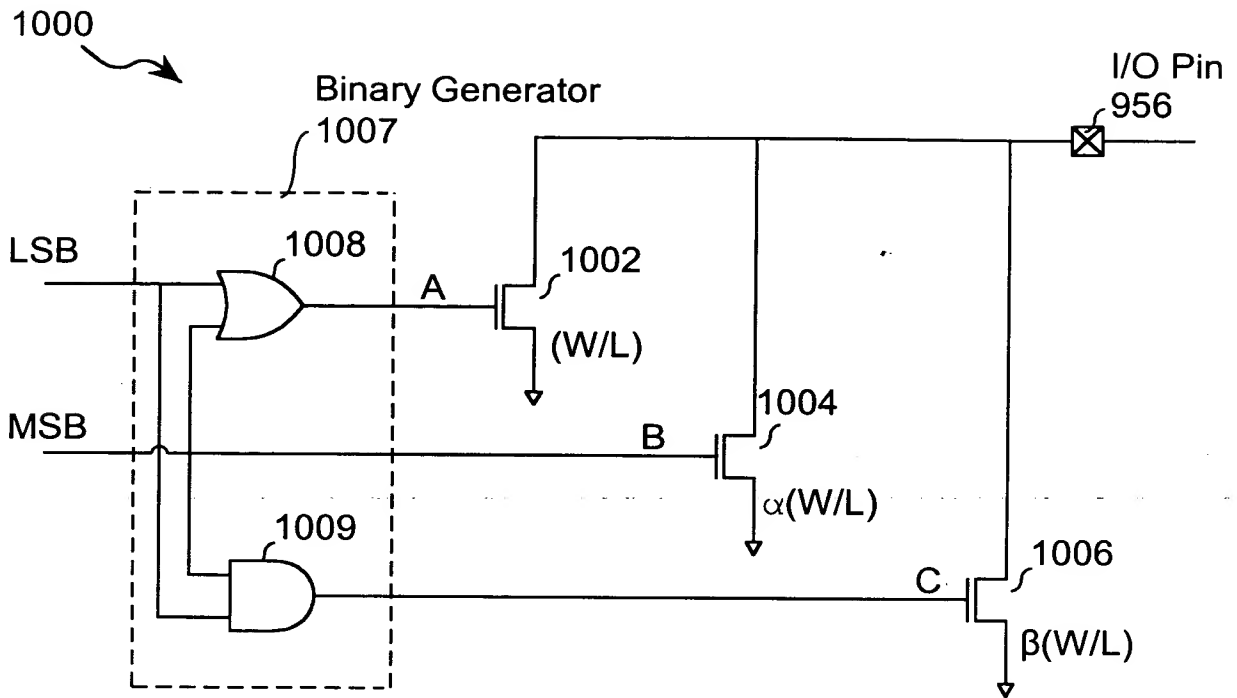
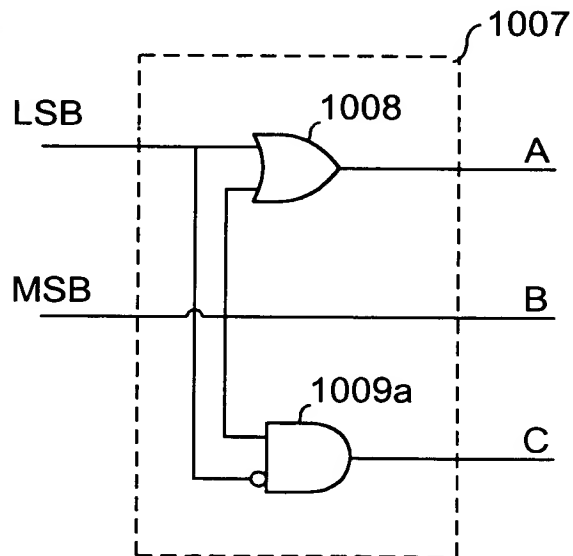


FIG. 32C

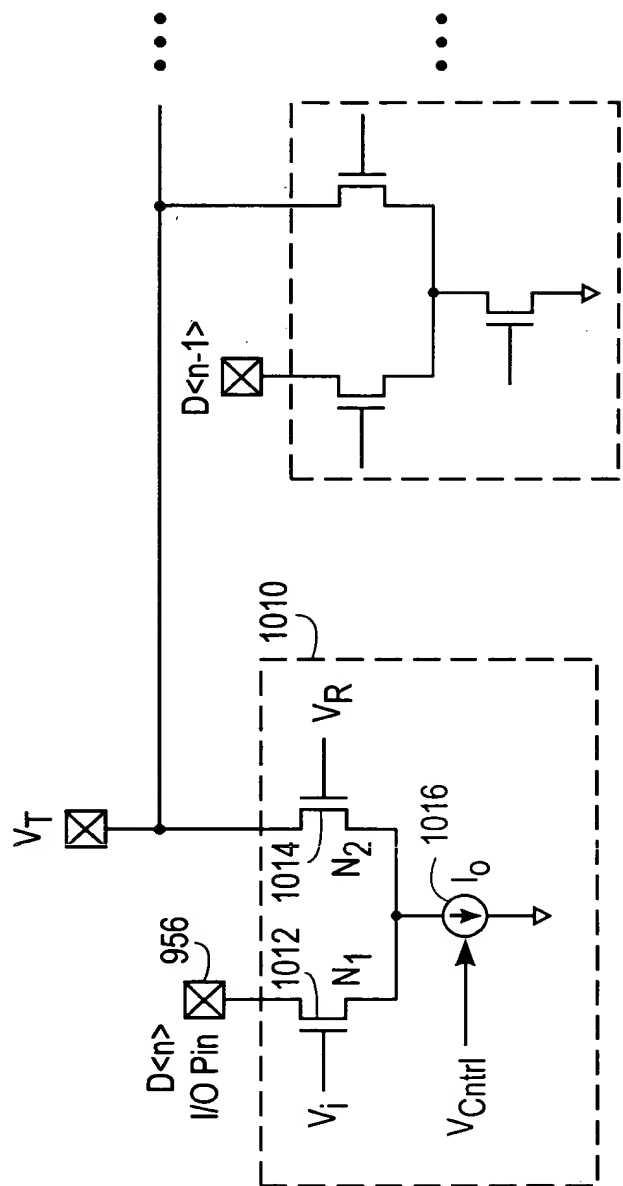


**FIG. 33A**



Gray Code Generator

**FIG. 33B**



Circuit to Reduce Switching Noise

FIG. 34

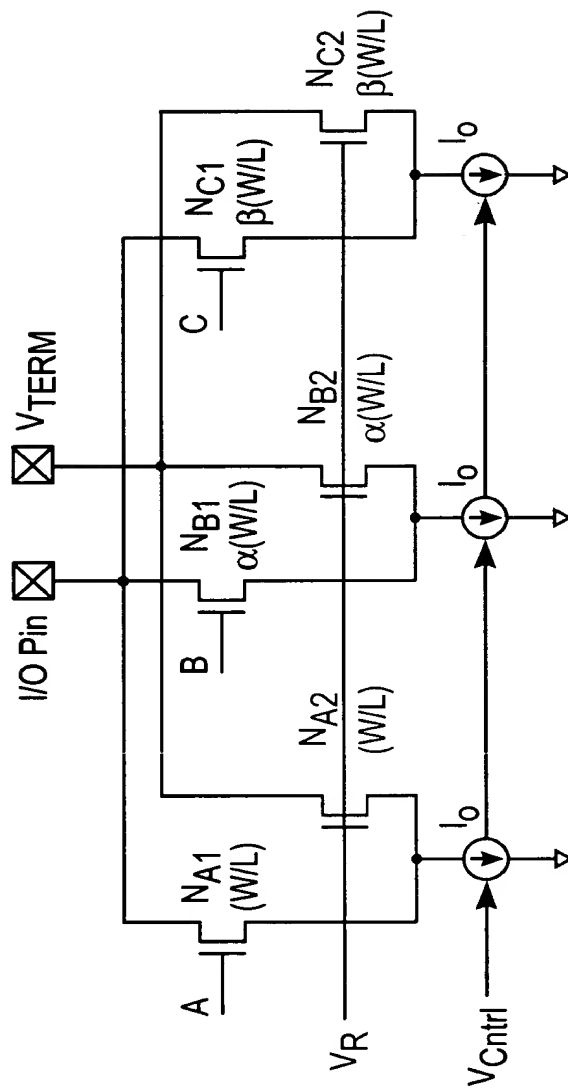
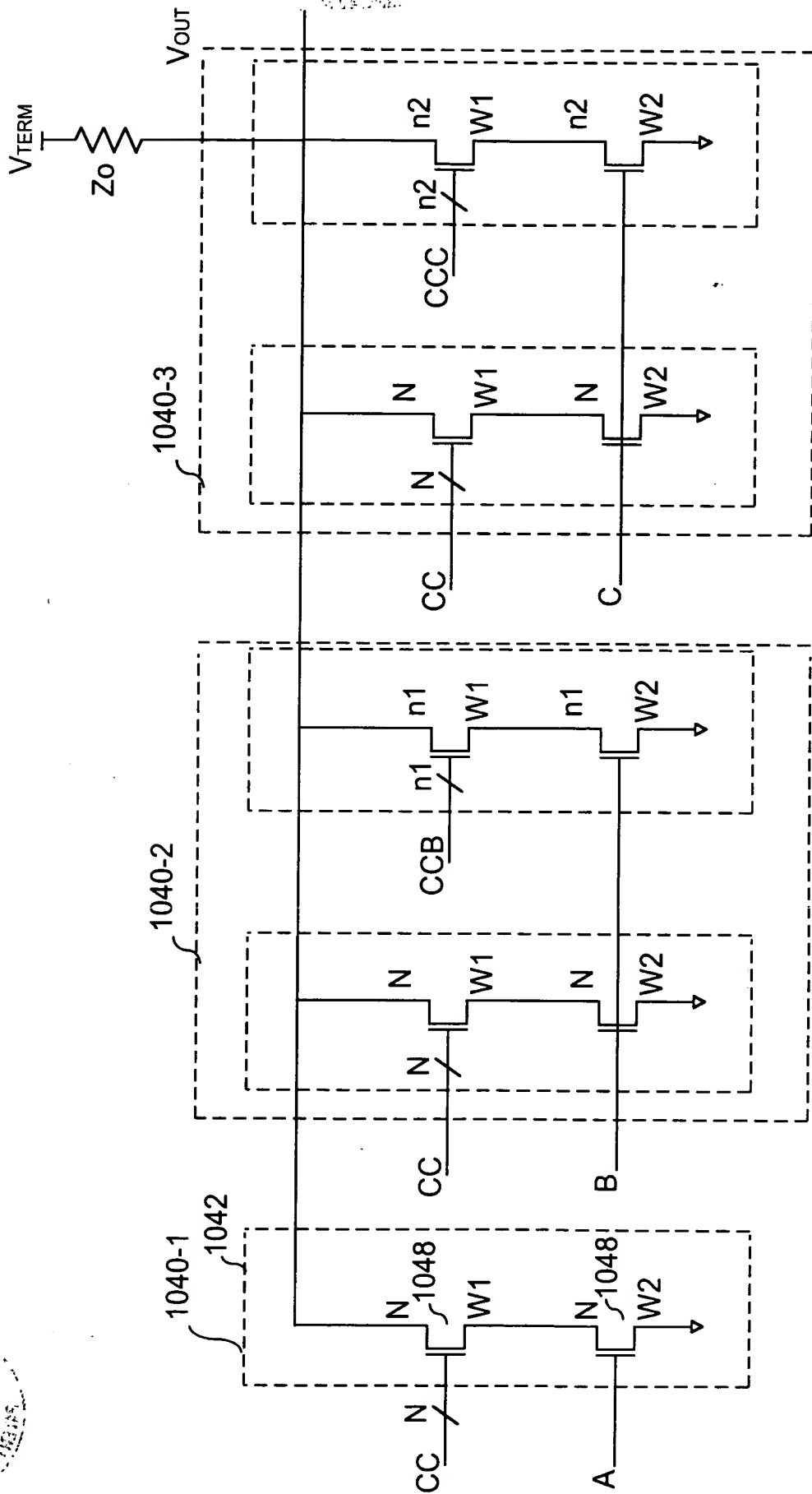


FIG. 35

FIG. 36



GDS Compensated Multi-PAM Output Driver with Current Control

**FIG. 37A**

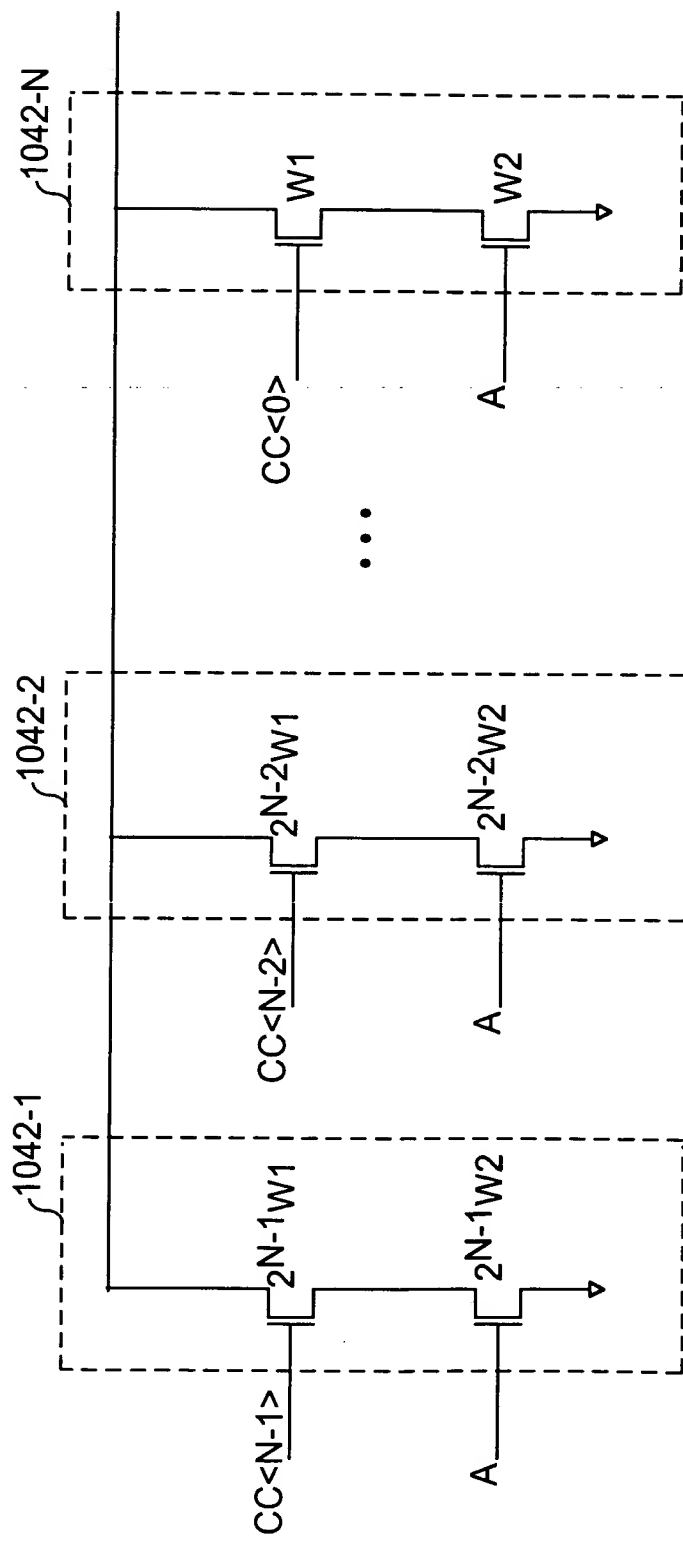
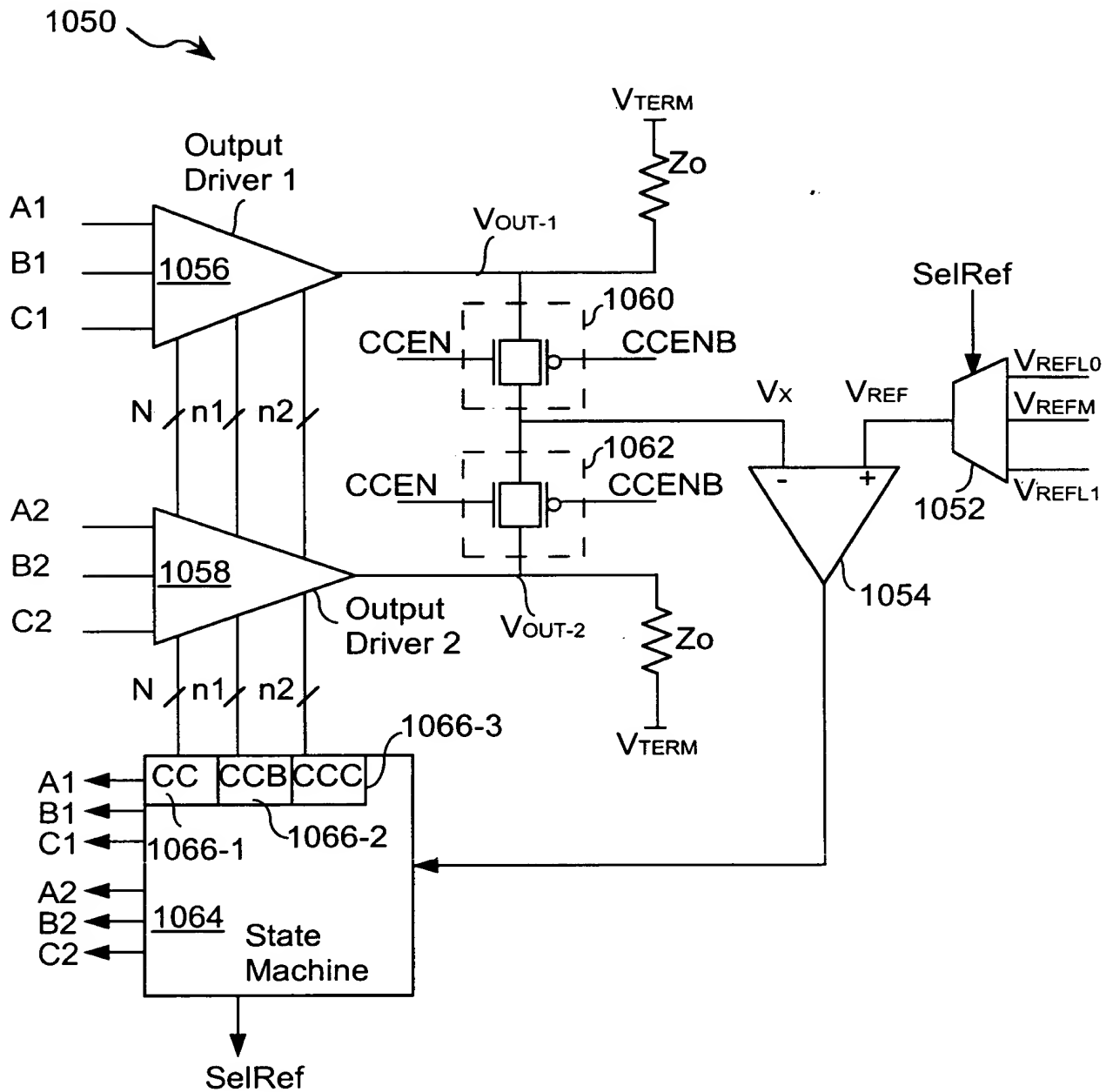


FIG. 37B

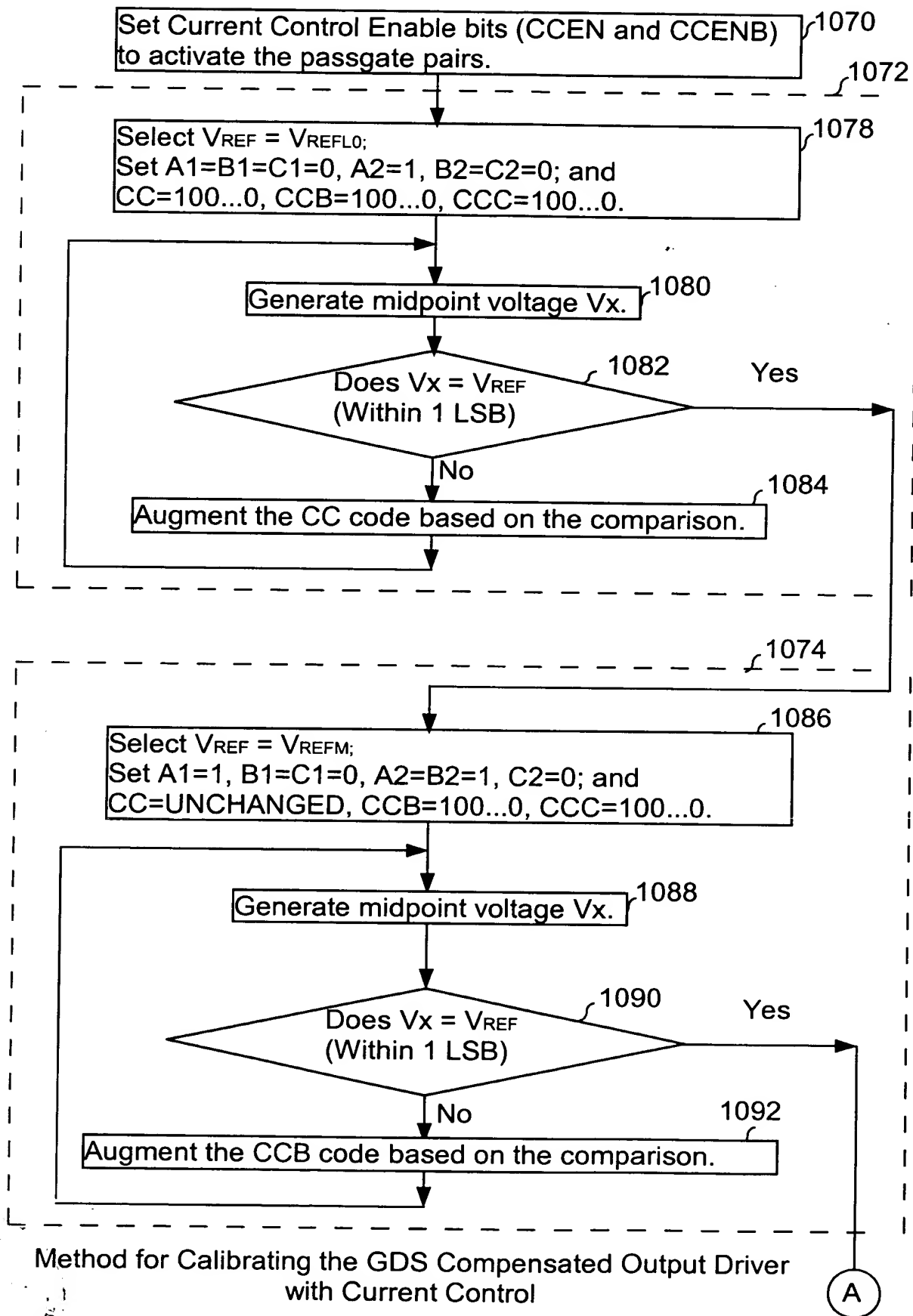




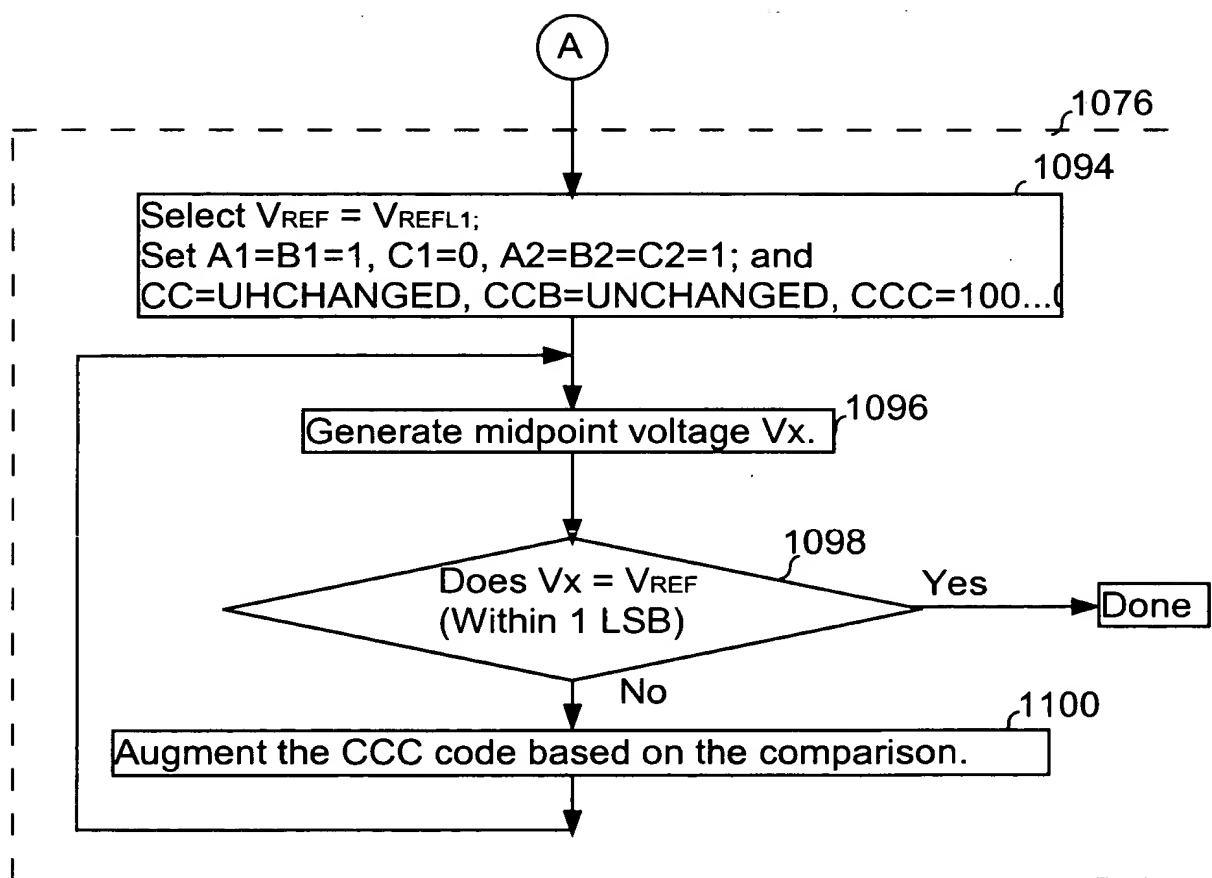
Circuit for Calibrating the GDS Compensated Output Driver  
with Current Control

**FIG. 38**





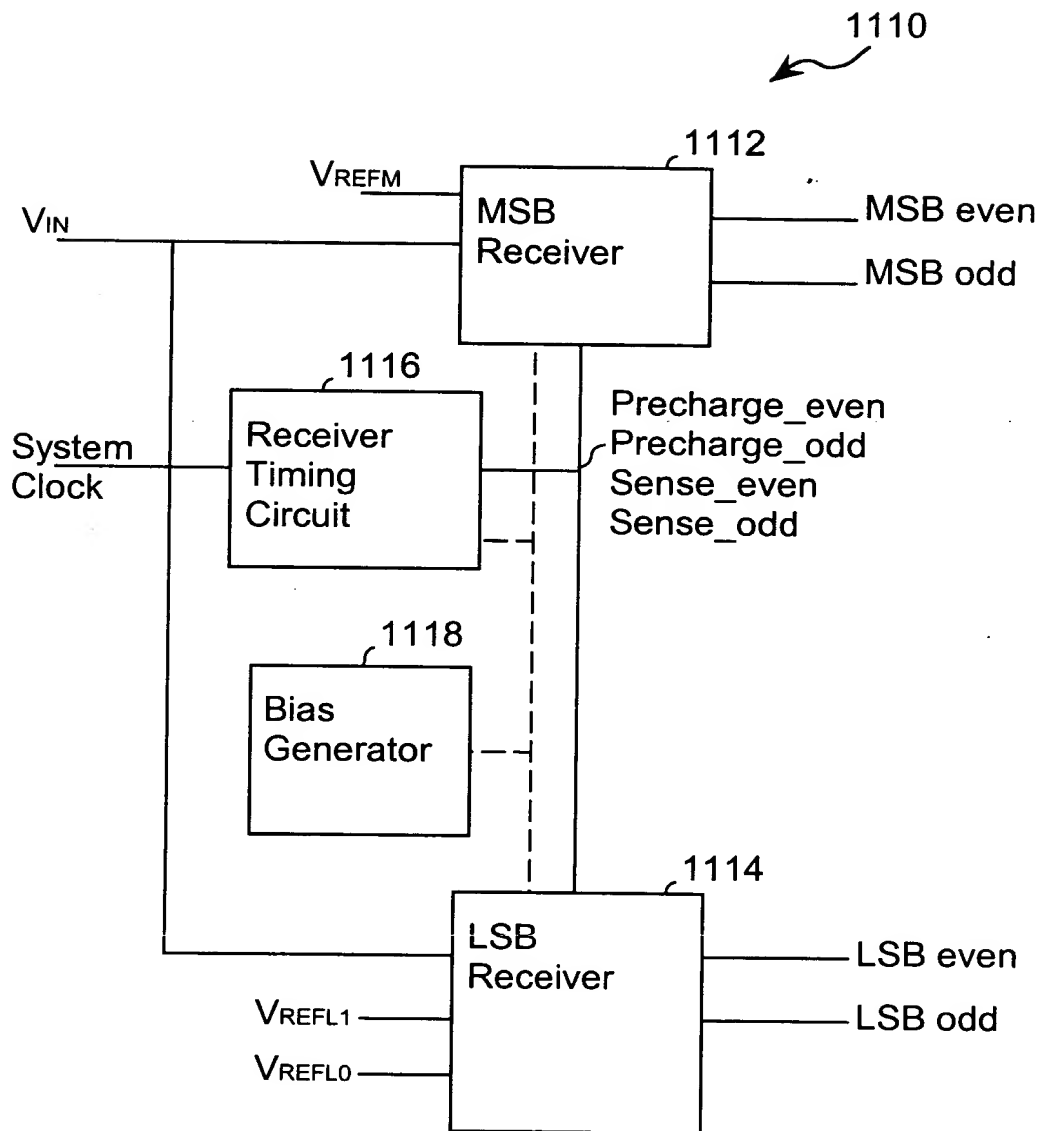
**FIG. 39A**



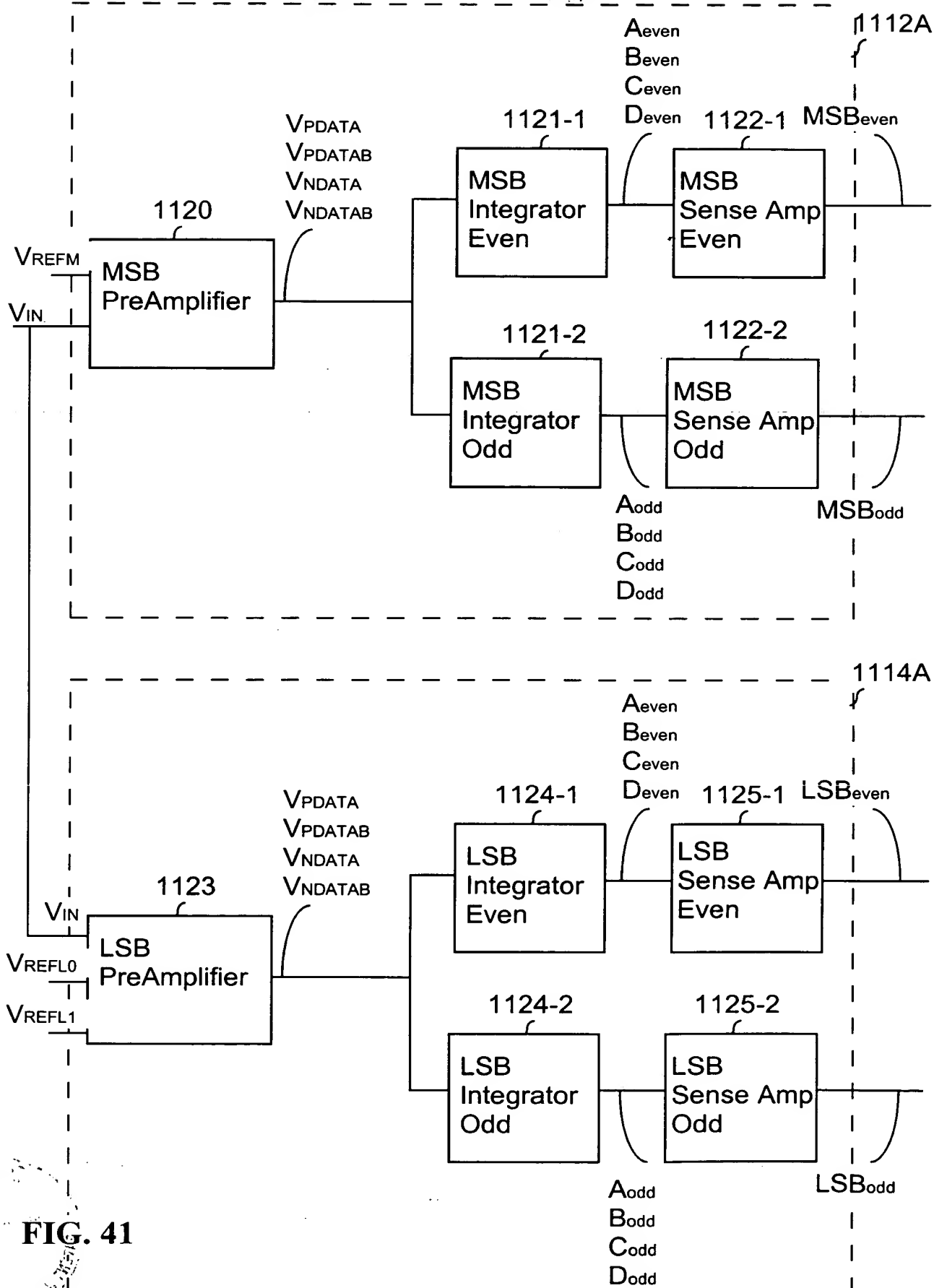
Method for Calibrating the GDS Compensated Output Driver  
with Current Control

**FIG. 39B**

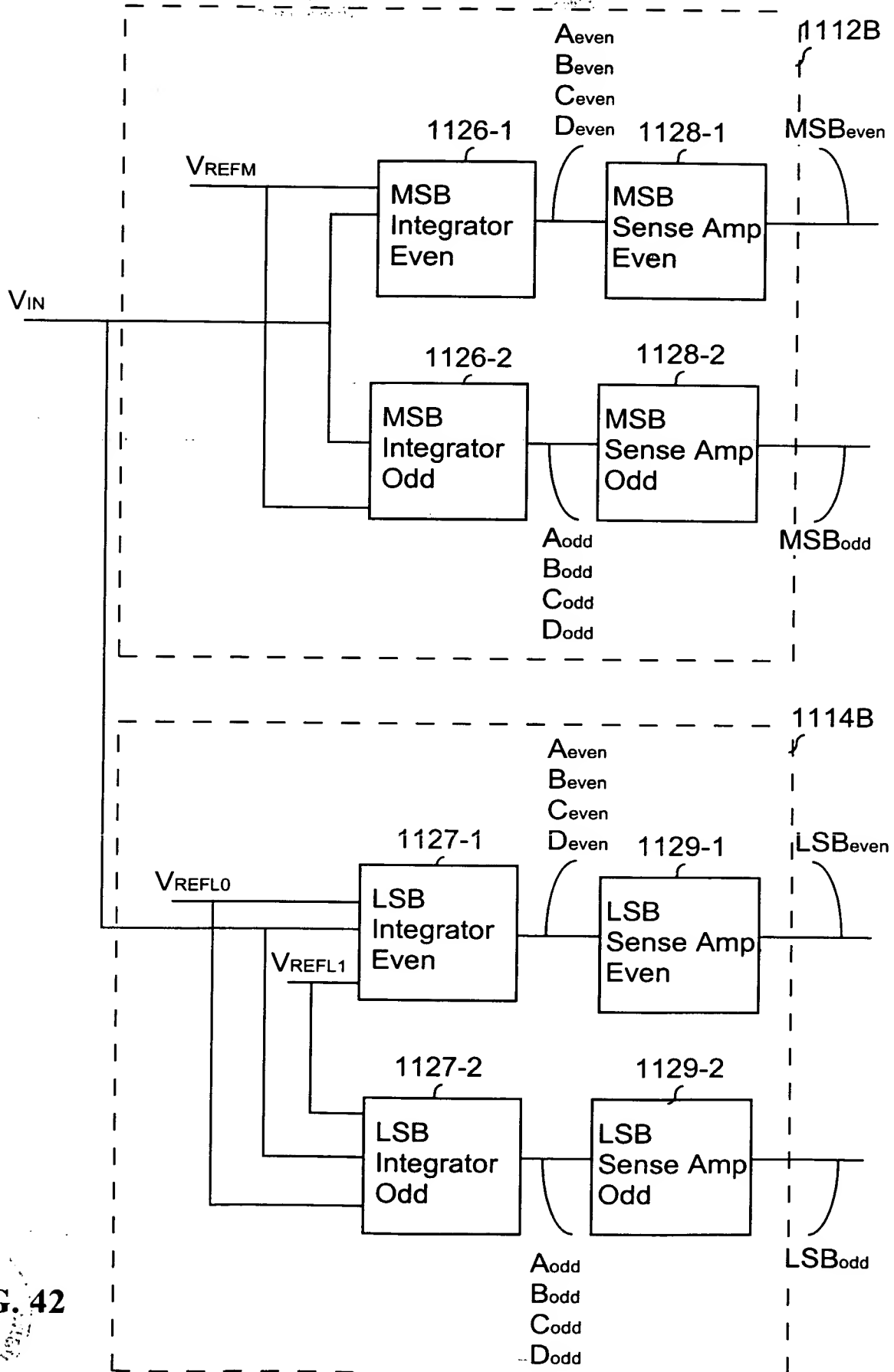




Multi-PAM Receiver  
**FIG. 40**

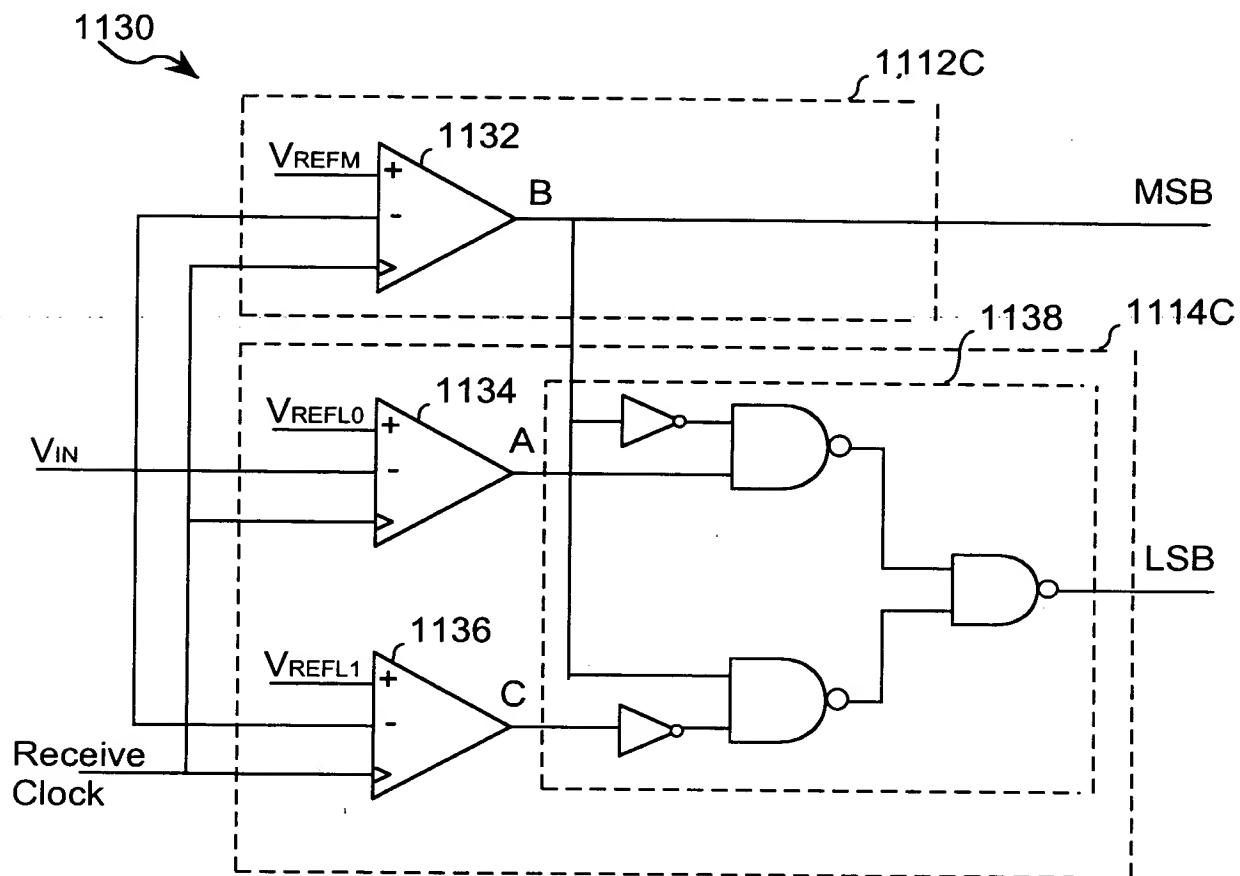


**FIG. 41**



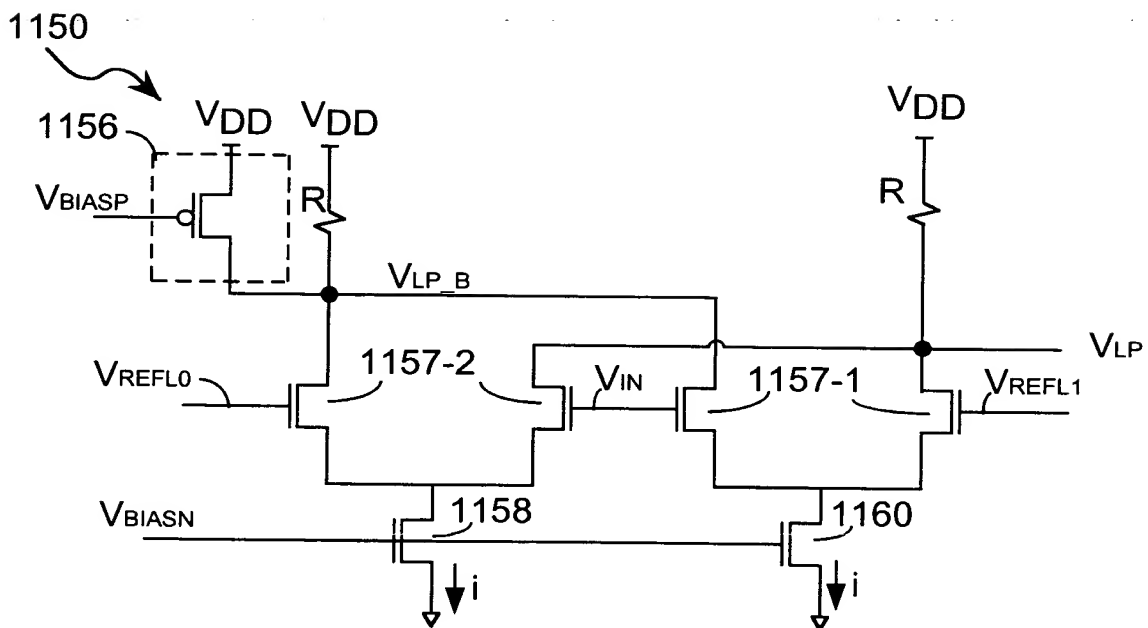
**FIG. 42**

# MULTI-PAM RECEIVER



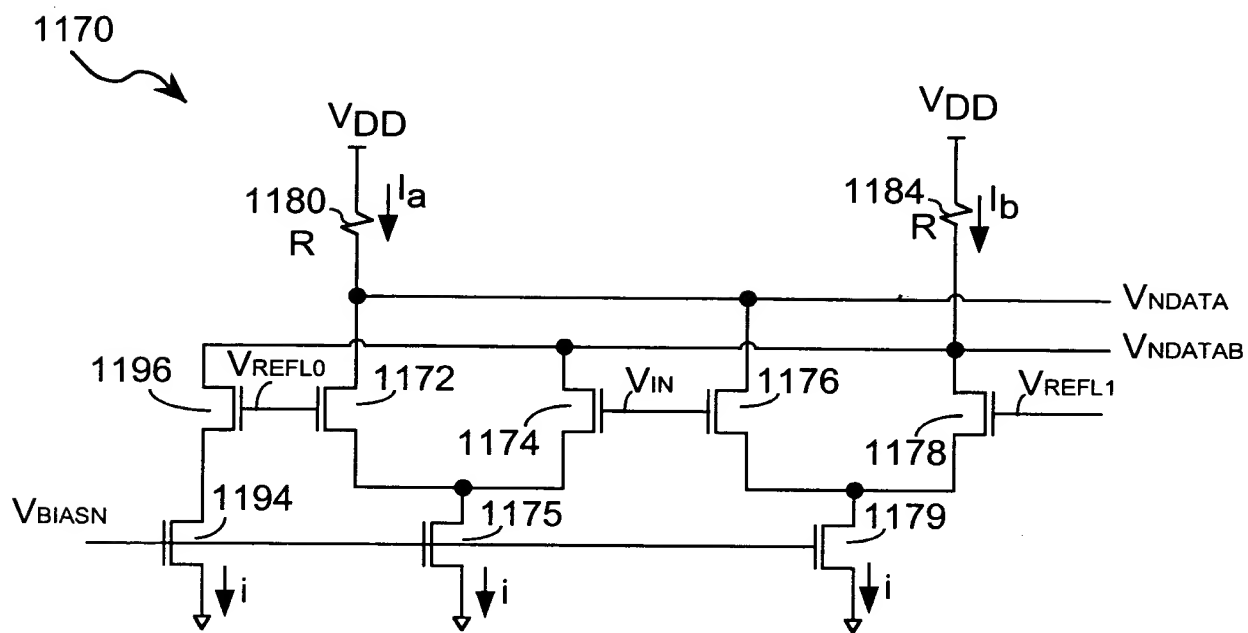
Multi-PAM Receiver

**FIG. 43**



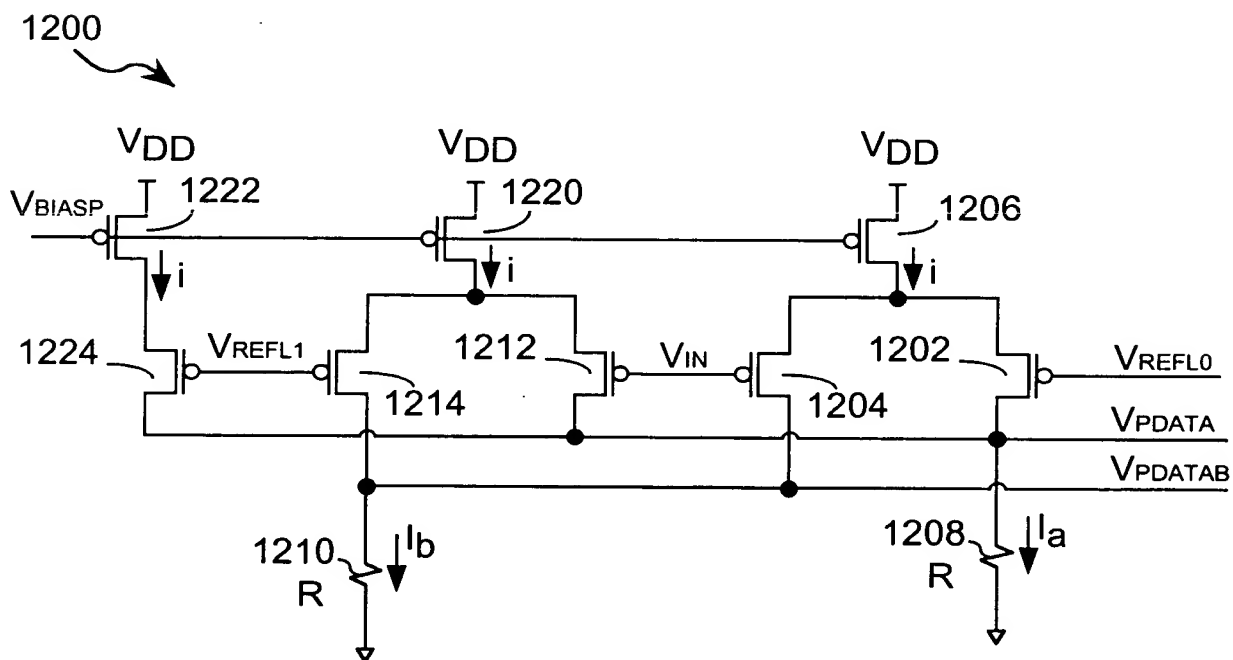
Multi-PAM Pre-Amplifier  
**FIG. 44**





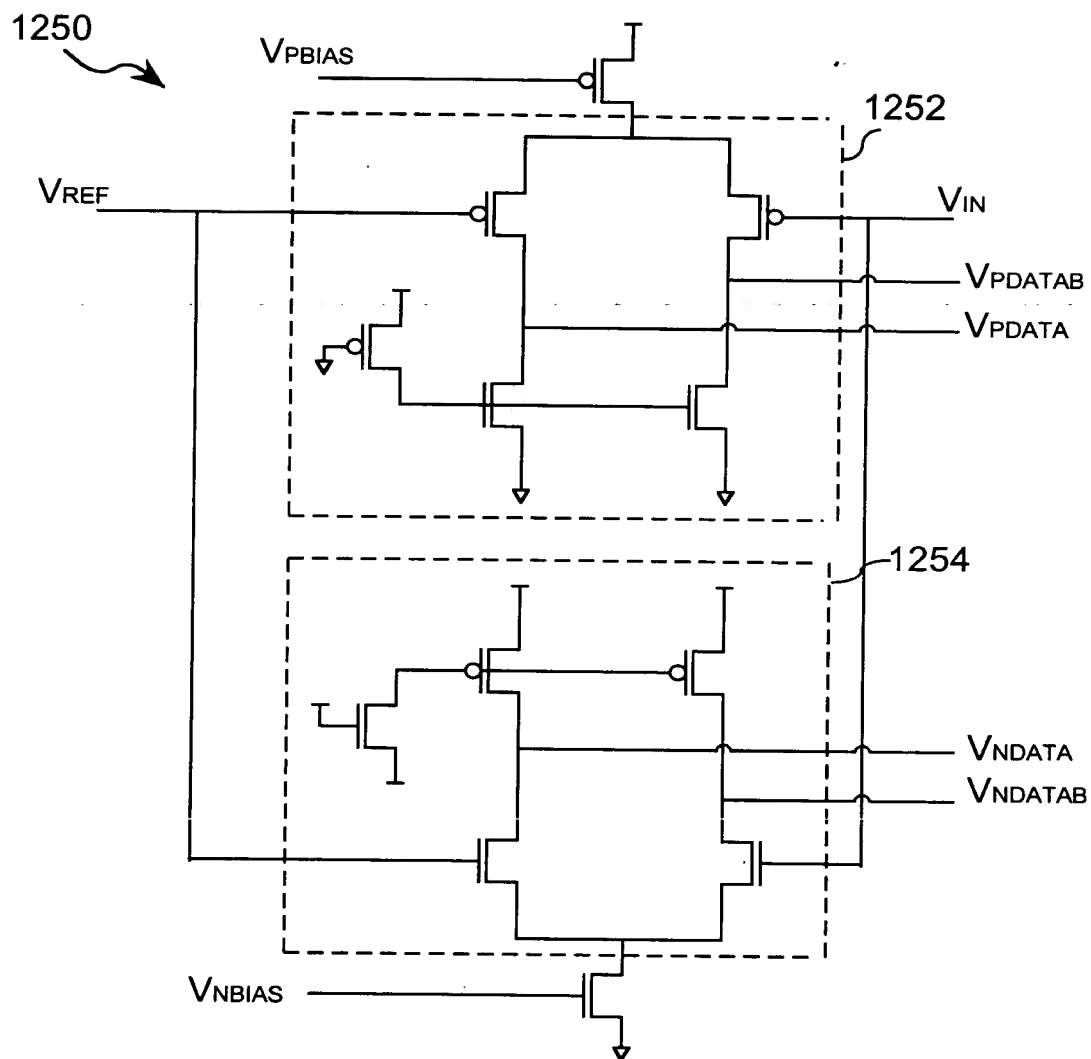
## Multi-PAM Pre-Amplifier

**FIG. 45A**



## Multi-PAM Pre-Amplifier

**FIG. 45B**

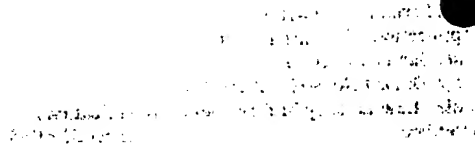


Multi-PAM Pre-Amplifier for MSB

**FIG. 46**



LSB F



**FIG. 47**

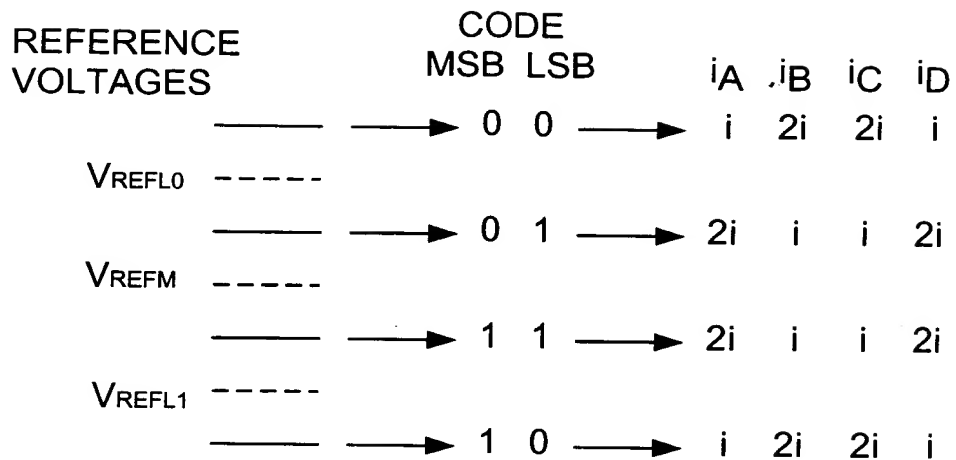


FIG. 48

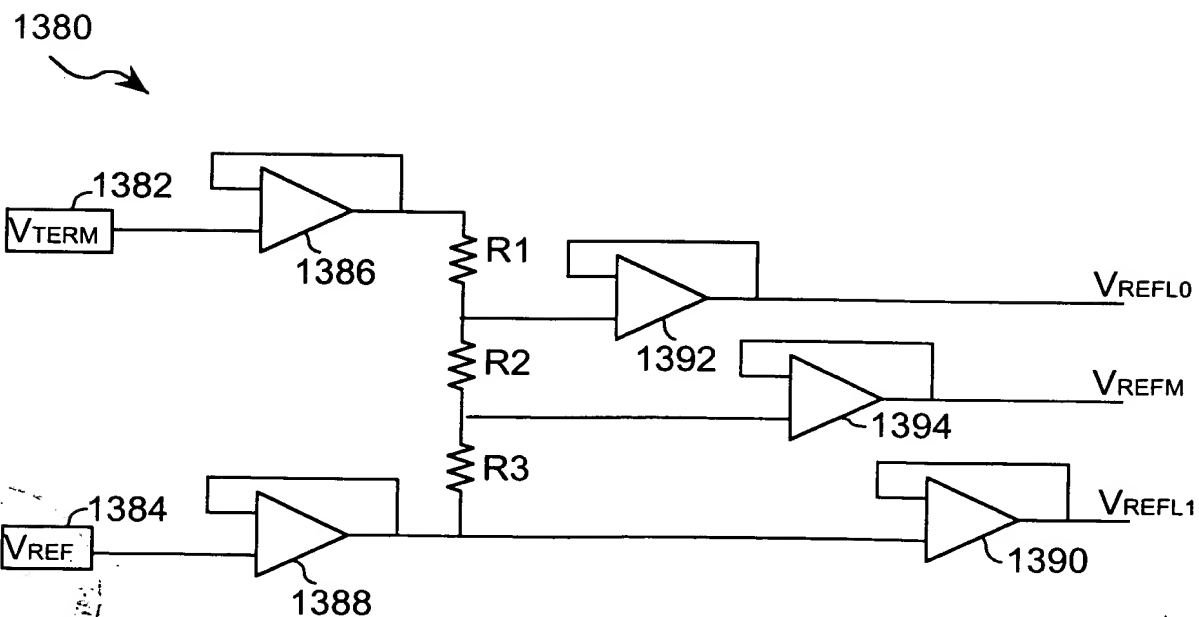


FIG. 49

# RECEIVER TIMING CIRCUIT

1116

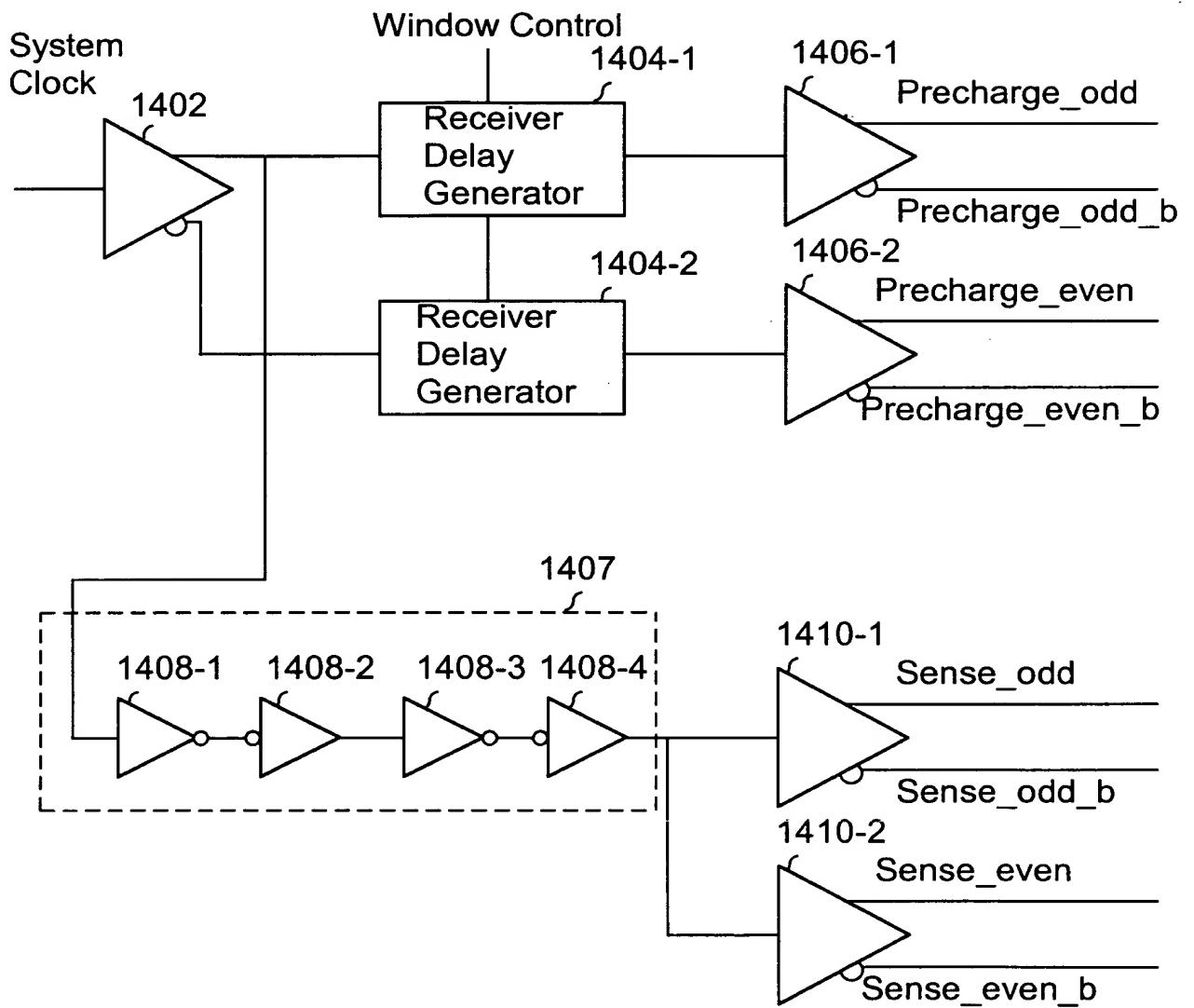
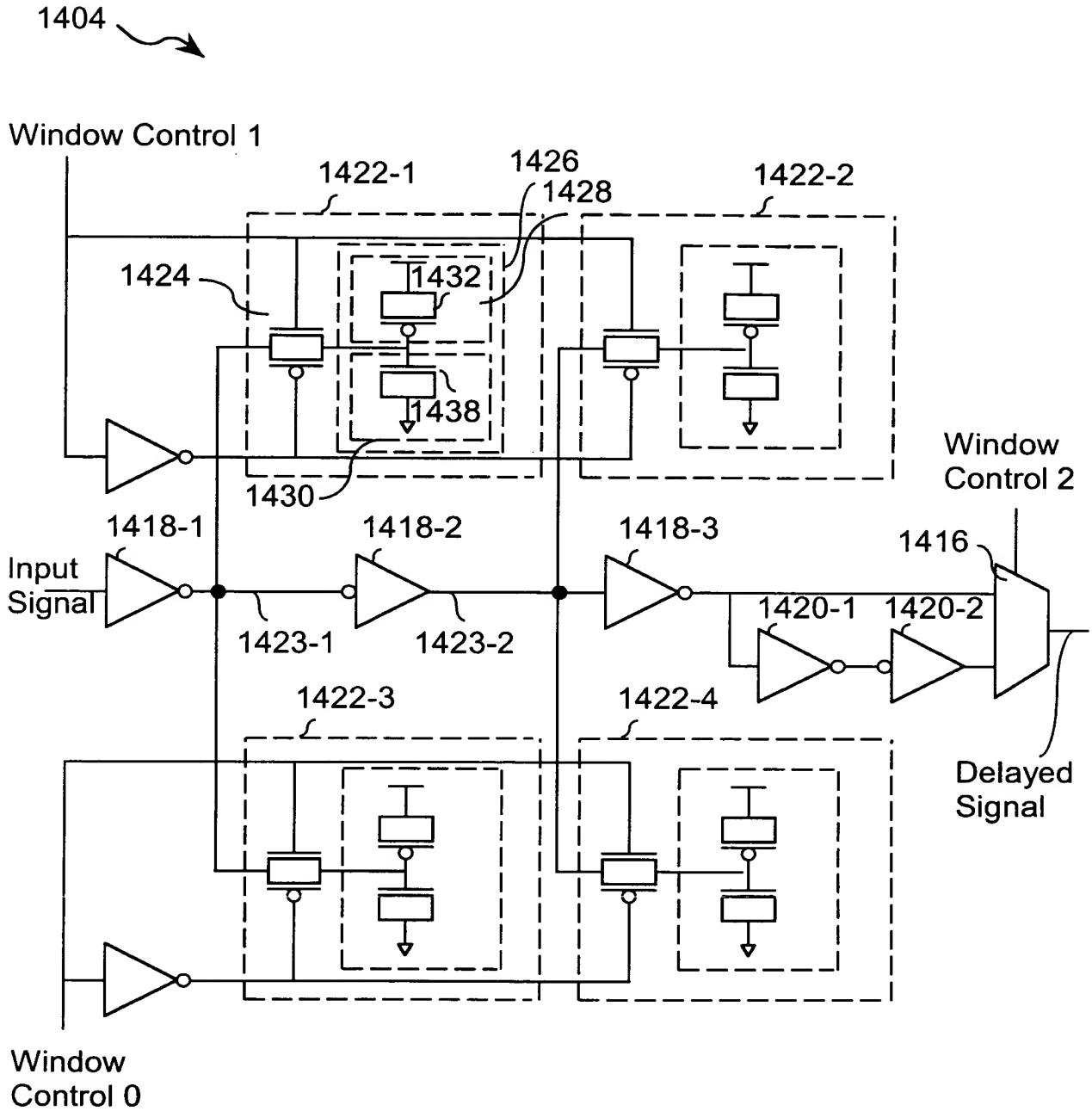


FIG. 50



Receiver Delay Generator

**FIG. 51**

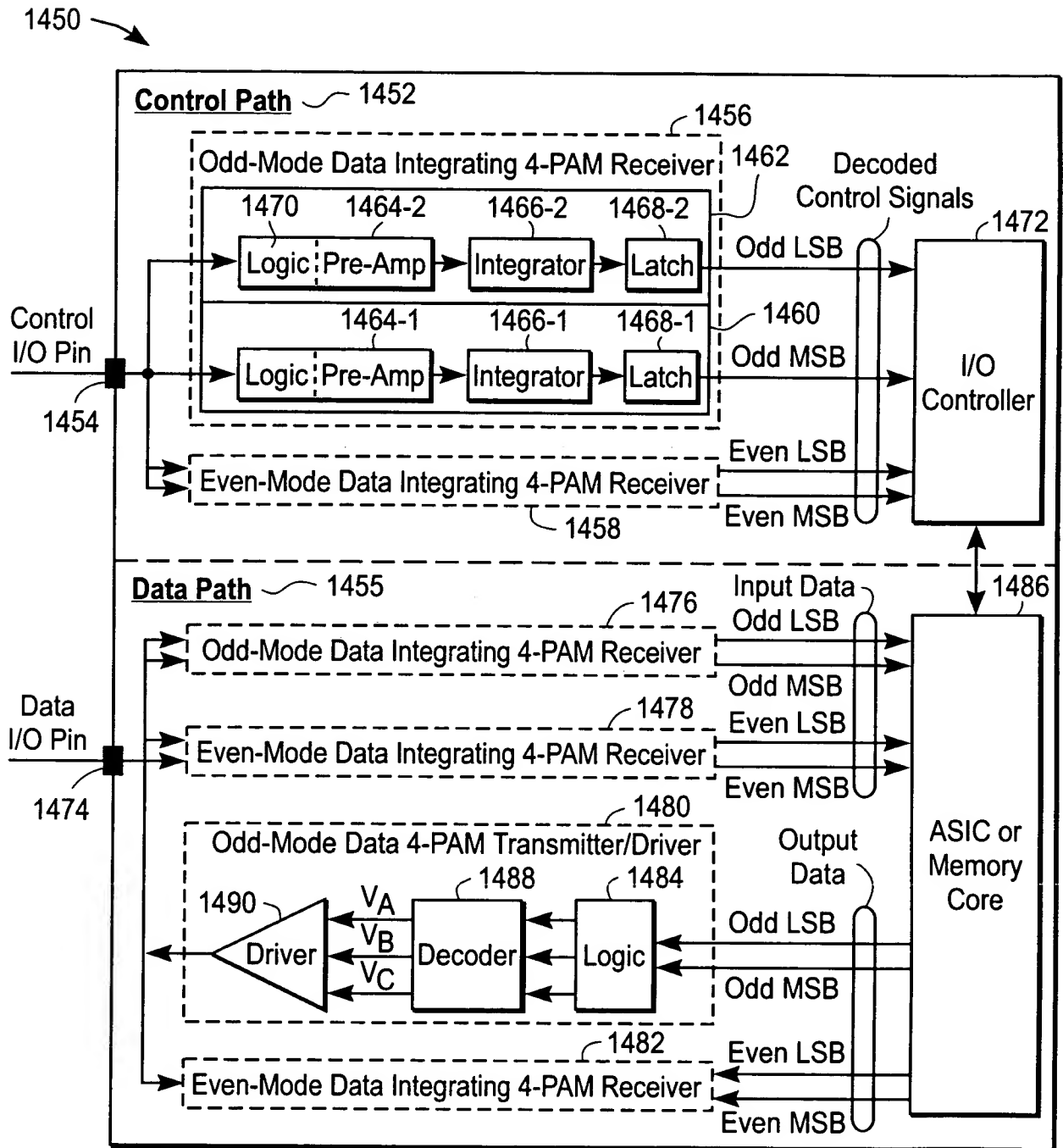


FIG. 52A

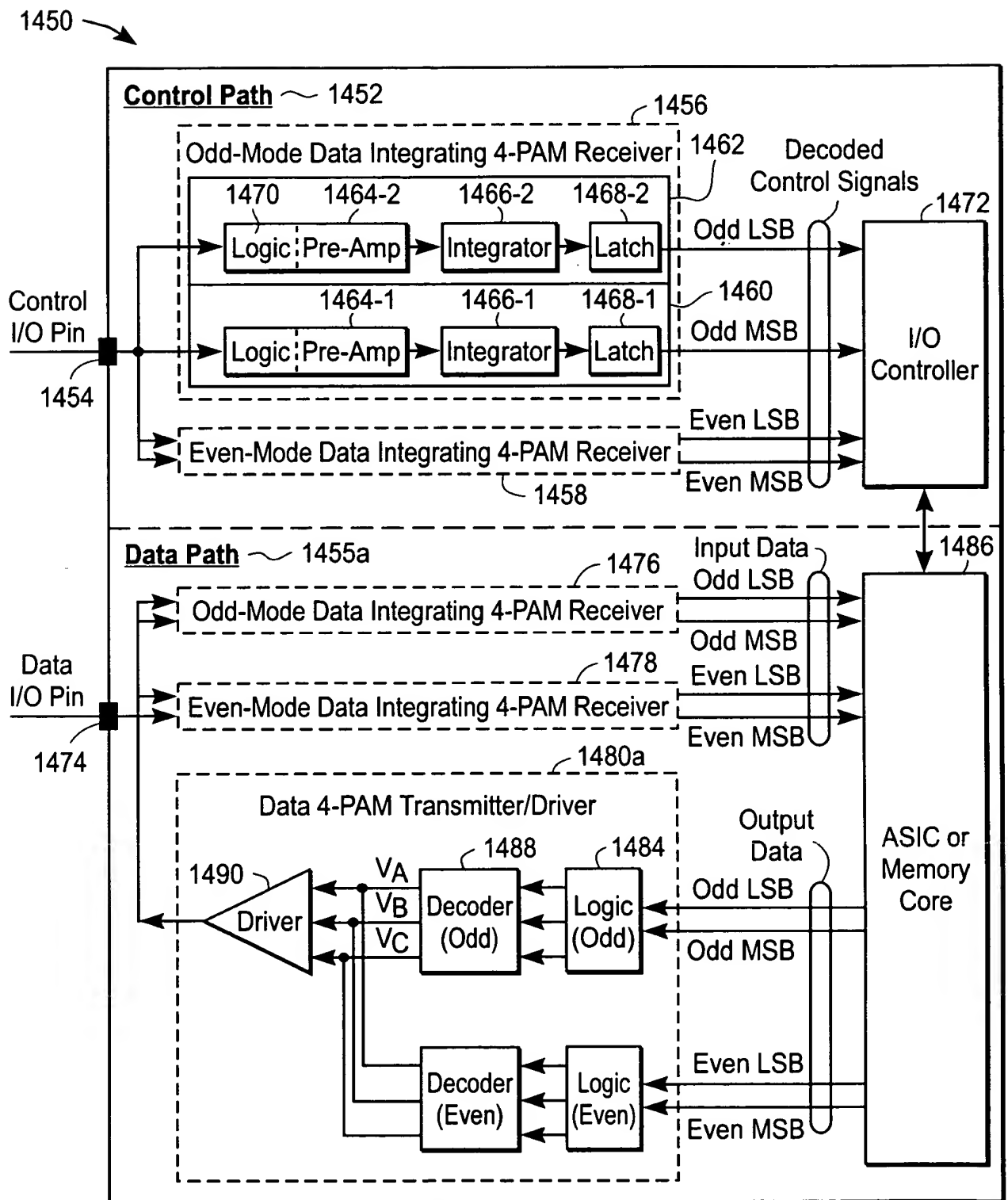
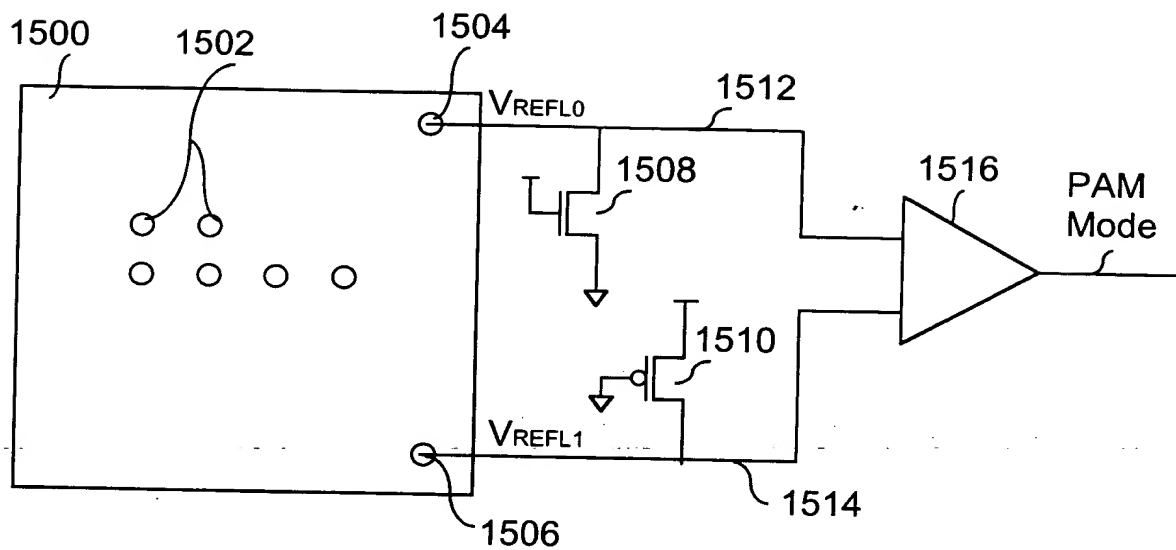
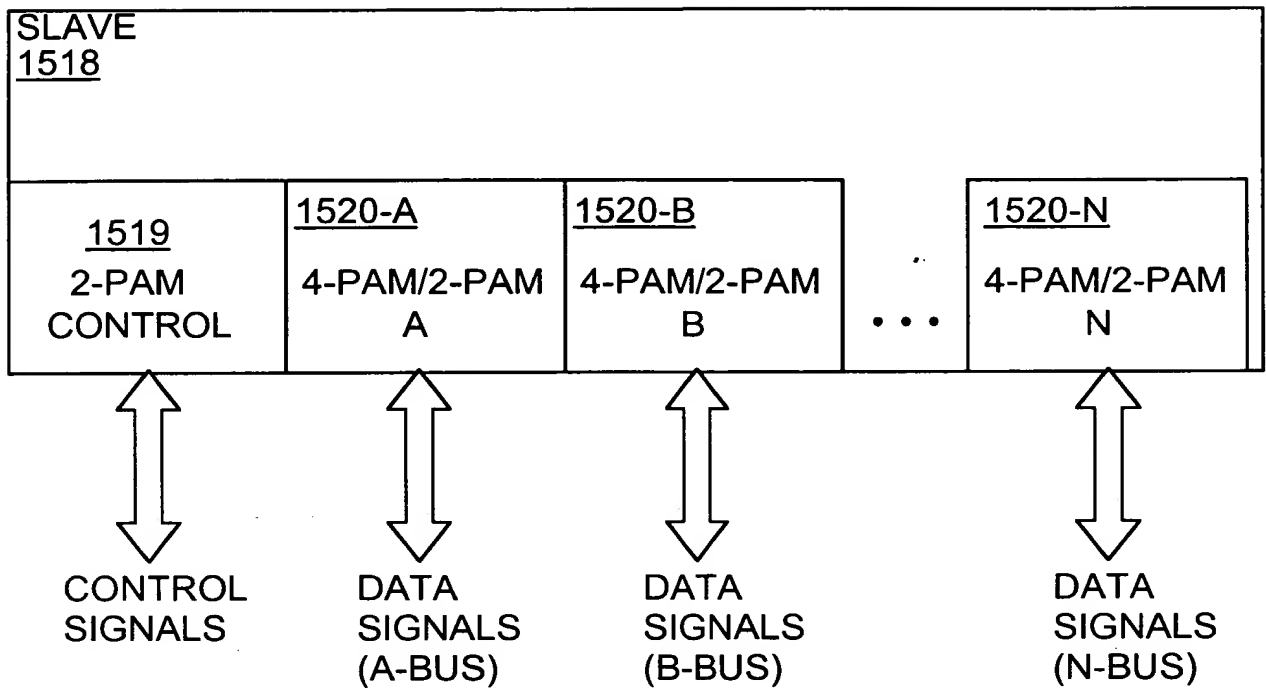


FIG. 52B

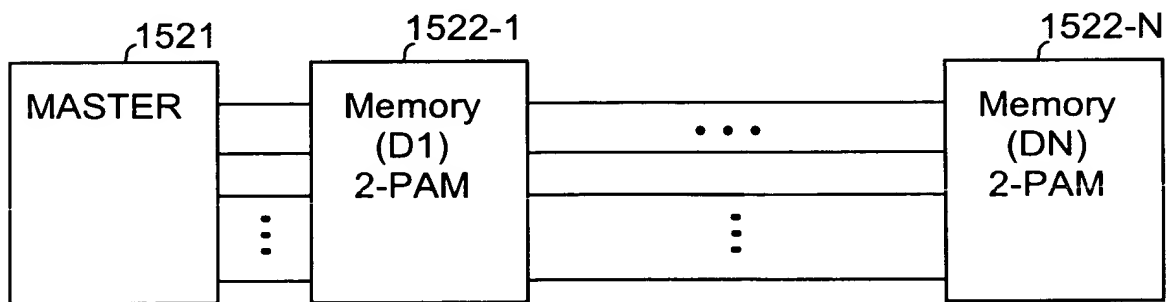


Automatic Detection of 2-PAM or 4-PAM Mode  
**FIG. 53**

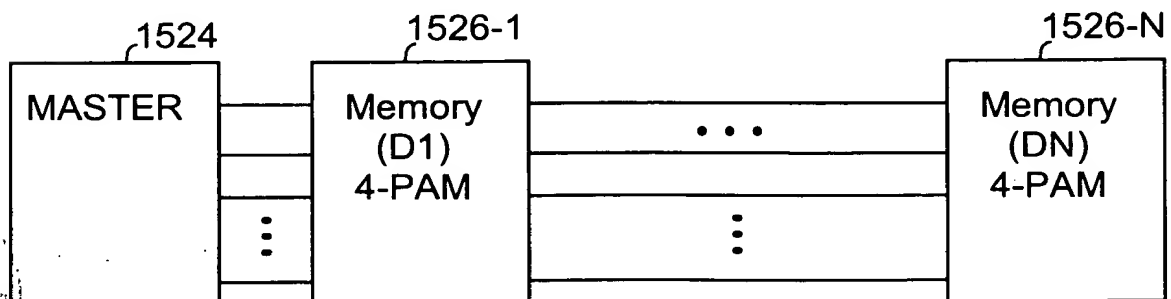




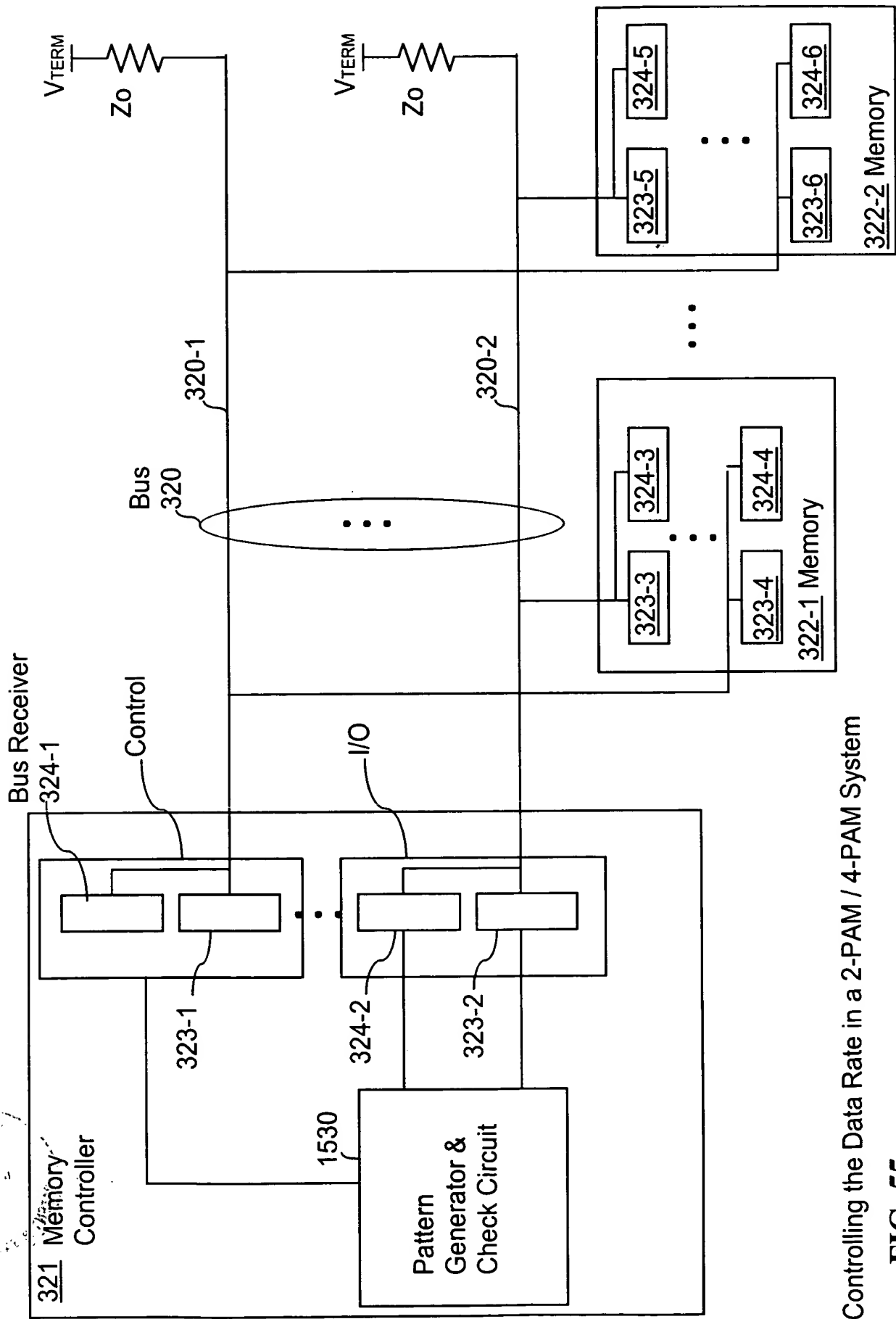
**FIG. 54A**



**FIG. 54B**

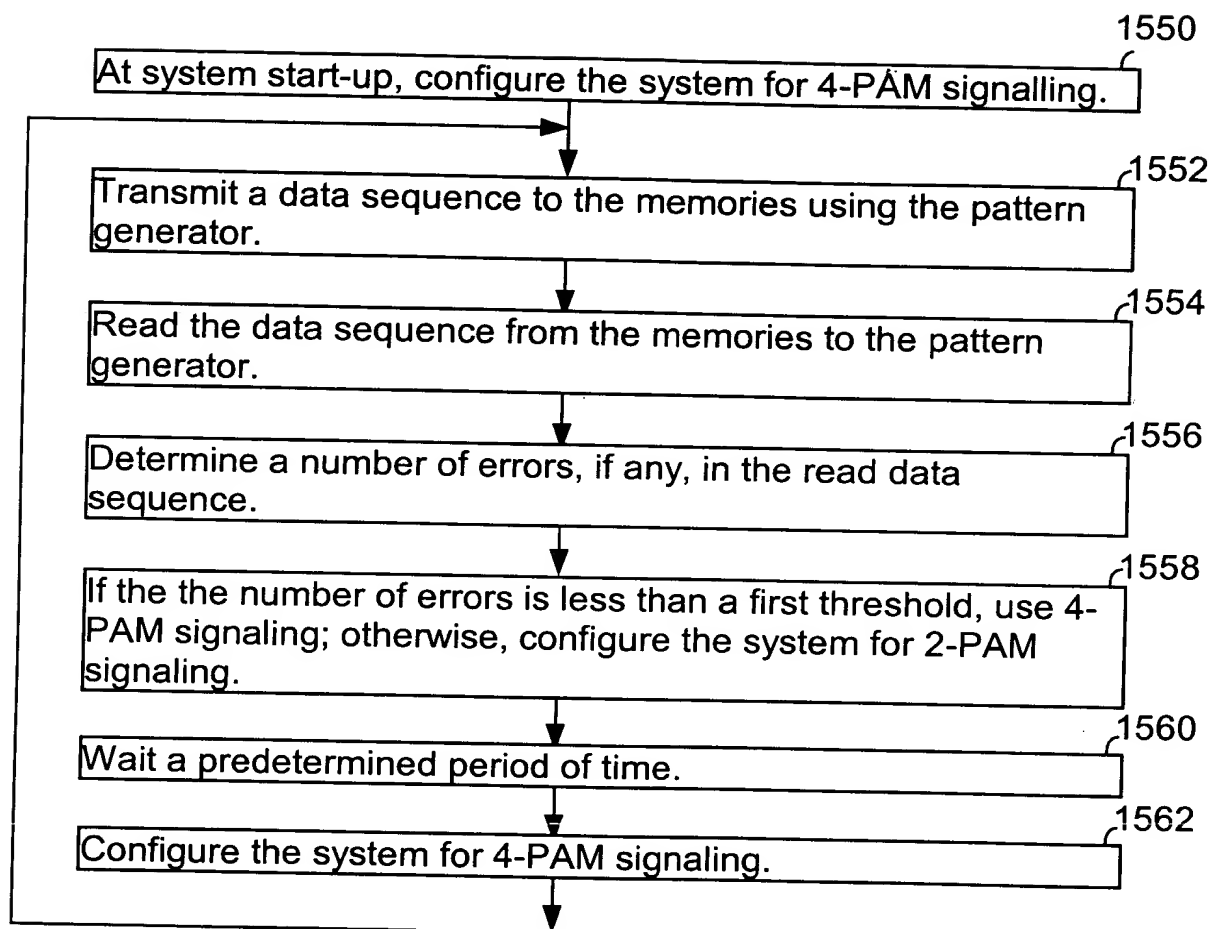


**FIG. 54C**



Controlling the Data Rate in a 2-PAM / 4-PAM System

**FIG. 55**



Method for Determining 4-PAM / 2-PAM Signalling as a  
Function of Error Rate

**FIG. 56**

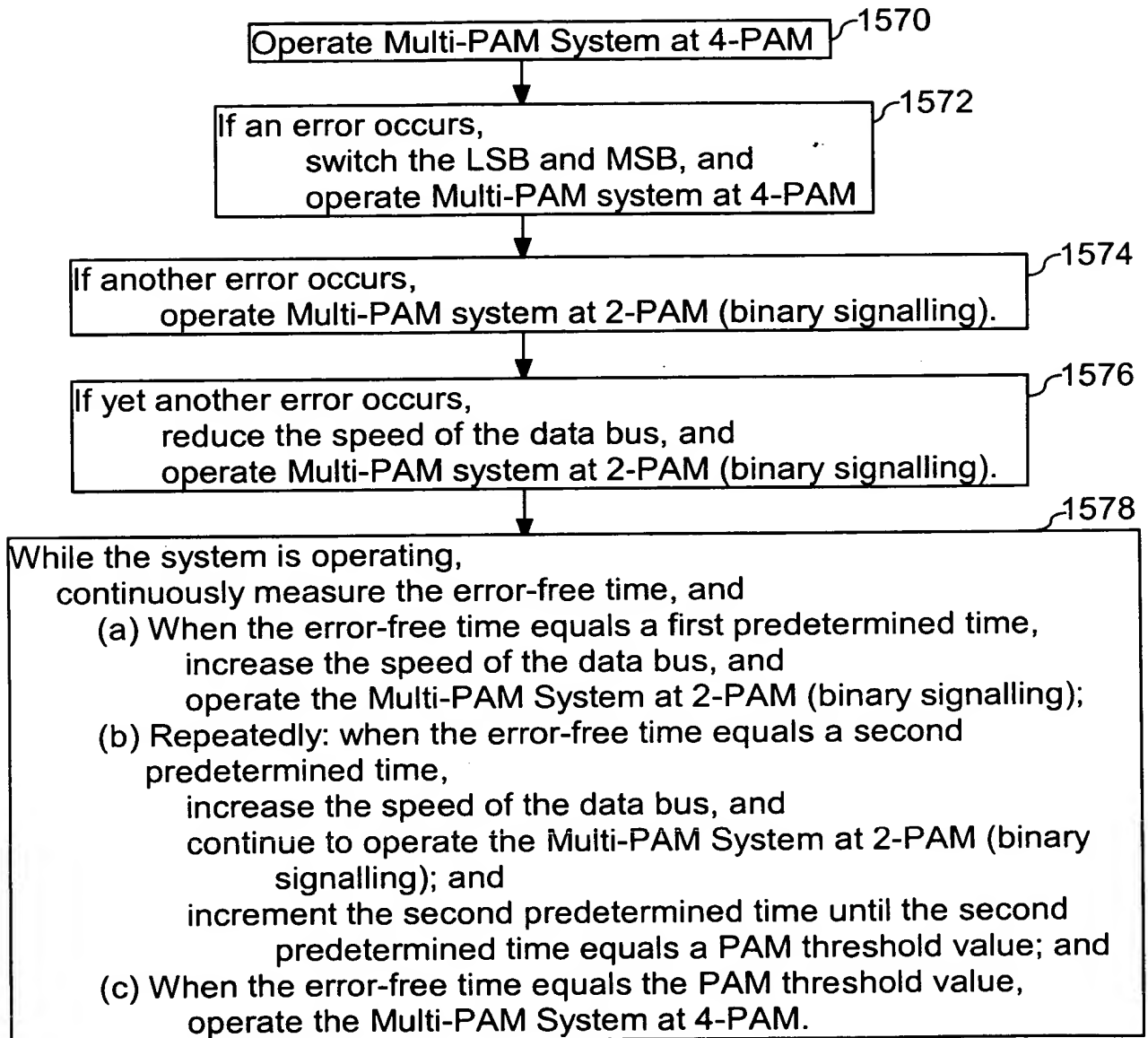
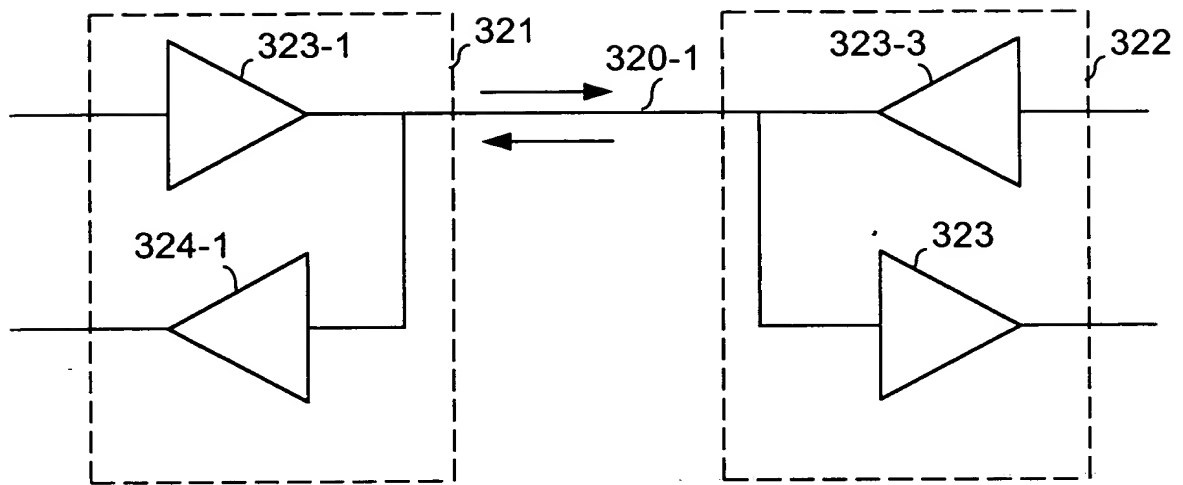
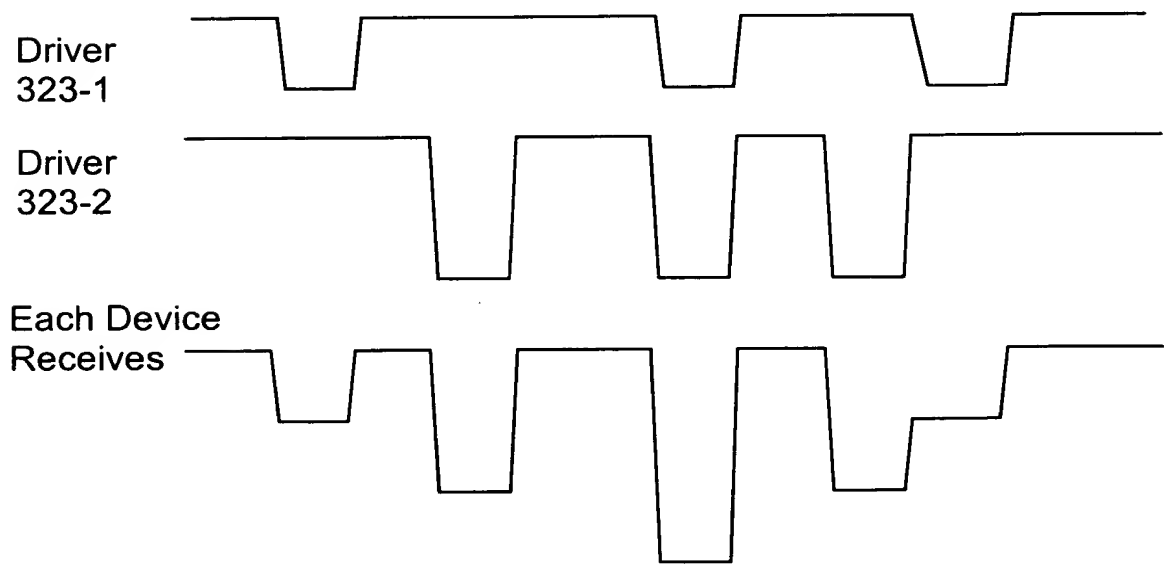


FIG. 57

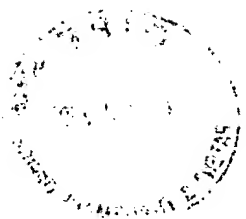




**FIG. 58**



**FIG. 59**



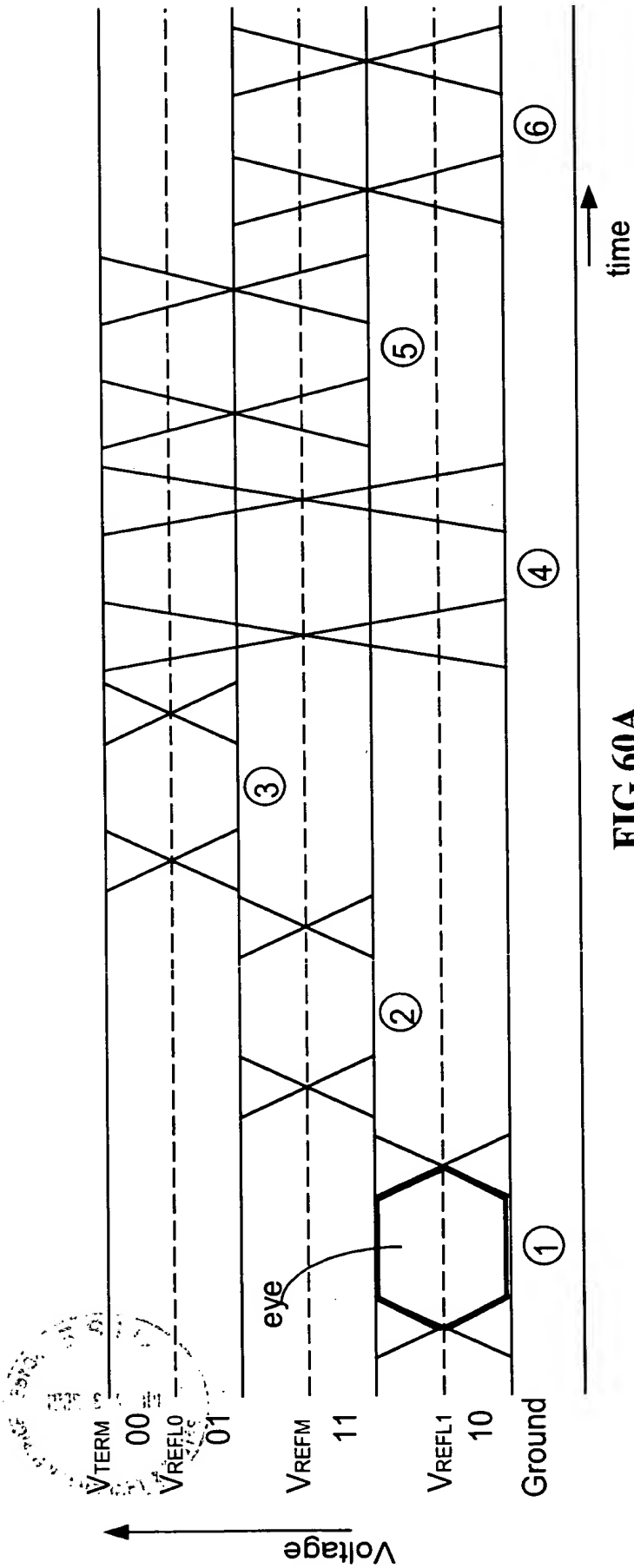


FIG. 60A

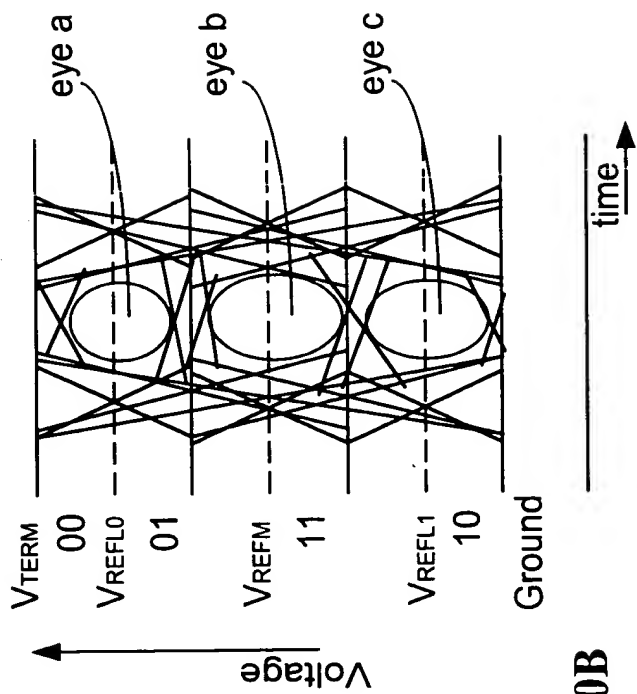


FIG. 60B